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Jussi Särkkä

A NOVEL METHOD FOR HAZARD RATE ESTIMATES OF THE SECOND LEVEL INTERCONNECTIONS IN INFRASTRUCTURE ELECTRONICS

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Academic dissertation to be presented, with the assent of the Faculty of Technology of the University of Oulu, for public defence in Raahensali (Auditorium L10), Linnanmaa, on June 19th, 2008, at 12 noon

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Abstract

Electronic devices are subjected to various usage environments, wherein stresses are induced to components and their interconnections. The level of stress affects the interval of failure occurrences. When the stress level and aging characteristics of sub-material parts are known, the failure occurrence can be predicted. However, the predictions are based on uncertainties and a practical method to help to assess the component interconnection reliability is needed.

In this thesis a novel method to utilize the accelerated stress test data for the hazard rate estimates is introduced. The hazard rate expectations of the interconnection elements are presented as interconnection failures in time (i-FIT) figures that can be used as a part of the conventional product reliability estimates. The method utilizes second level reliability test results for a packaging type specific failure occurrence estimates. Furthermore, the results can be used as such in the component packaging reliability estimates.

Moreover, a novel method to estimate the interconnection failures in terms of costs is presented. In this novel method the interconnection elements are dealt as cost elements. It is also shown that the costs of the interconnection failures could be very high, if the stress-strength characteristics of the interconnection system are wrongly chosen.

The lead-free manufacturing has emphasized the thermal compatibility of the materials of the component, the solder and the Printed Wiring Board. Improper materials for Area Array components will result as excessive component warping during the reflow, as is shown in this thesis. A novel method for estimating the amount of component warping during the lead-free reflow is introduced.

In this thesis, a method to predict the second level interconnection hazard rate is introduced. The method utilizes the second level reliability test data in the life time predictions of the component solder joints. The resulted hazard rates can be used as a part of product field performance estimates. Also, the effect of the process variation and the material properties on the lead-free solder joint reliability is introduced.

Keywords: component warpage, FIT, hazard rate, lead free electronics, reliability estimation, solder joint failure, solder joint fatigue, solder joint reliability

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Tiivistelmä

Elektronisen laitteen materiaalien yhteensopivuus ja käyttöympäristö määrittävät sen kokemat rasitukset. Laitteen komponentteihin tai niiden liitoksiin kohdistuvat rasitukset aiheuttavat lopulta laitteen vikaantumisen. Vikaantumisten taajuuteen vaikuttavat paitsi rasituksen taso ja tyyppi, myös laitteen materiaalien ominaisuudet. Todellinen vikaantumistaajuus perustuu kuitenkin muihinkin parametreihin, mistä johtuen vikaantumisennusteet voivat olla epätarkkoja. Tästä syystä käytännölliselle liitosten vikaantumisen arviointimenetelmälle on tarve.

Tässä väitöskirjassa esitellään uusi komponenttien juotosliitosten arviointimenetelmä, jonka avulla voidaan muuntaa kiihdytetyn rasitustestauksen tulos vikaantumistaajuusarvioksi laitteen todellisessa käyttöympäristössä. Menelmässä hyödynnetään levytason rasitustestauksen tuloksia komponenttien kotelotyyppikohtaisiin vikaantumisennusteisiin. Menetelmää voidaan käyttää sellaisenaan arvioitaessa komponenttikoteloiden luotettavuutta todellisissa rasitus- tai tuoteympäristöissä.

Väitöskirjassa esitellään myös uusi menetelmä vikaantuneiden liitosten kustannusten määrittämiseen, mikä auttaa myös uuden liitosteknologian kokonaiskustannusten arvioimisessa. Lisäksi väitöskirjatyössä osoitetaan, että liitosvikojen aiheuttamat kustannukset voivat olla erittäin korkeita, mikäli juotosliitoksiin kohdistuvat rasitukset ylittävät liitosten suunnitellun kestävyyden.

Elektroniikan lyijyttömän valmistamisen myötä komponenttien, juotteen ja piirilevyn materiaalien yhteensopivuus korostuu. Väitöskirjatyössä osoitetaan, että yhteensopimattomien materiaalien käyttäminen komponenteissa voi johtaa komponentin liialliseen taipumaan kuumakonvektiojuottamisen aikana. Lisäksi esitellään menetelmä komponentin taipuman arvioimiseksi lämpötilan funktiona.

Tässä väitöskirjassa esitellään uusi menetelmä, jolla voidaan arvioida komponenttien juotosliitosten vikaantumista ja vikaantumisen vaikutusta tuotteiden kokonaiskustannuksiin. Menetelmä perustuu kiihdytetyn rasitustestauksen tuloksiin, joita voidaan käyttää juotosliitosten vikaantumisten arvioimiseen tuotteen todellisissa käyttöolosuhteissa. Lisäksi väitöskirjatyössä on arvioitu juotosmateriaalin ja juotosaluemitoituksen vaikutusta juotosliitosten luotettavuuteen.

Asiasanat: juotosliitosten luotettavuus, juotosliitosten vikaantuminen, vikataajuus, luotettavuusennusteet, lyijytön elektroniikka, komponentin taipuminen

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Kiiminki, April 2008 Jussi Särkkä

"*We can't solve problems by using the same kind of thinking as we used when we created them.*"
"*Education is what remains after one has forgotten everything he learned in school.*"

—Albert Einstein

List of symbols and abbreviations

A	effective solder joint area, 2/3 of solder wetted area
A.F.	Acceleration Factor
$A.F._{SDNL}$	Acceleration Factor, Stress Dependent Norris-Lanzberg relation
A_s	material constant
B_s	material constant
c	fatigue ductility exponent
C,C(t)	cost of failures
c_{SPC}	cost of product, Standard Product Cost
C_{pf}	proportionality factor
corr (ΔT)	stress dependent correction term
D	dual, or dual in line configuration
E	Young's modulus
f	frequency of cycles
F, F(t)	failure function, unreliability
F_u	unideality factor
h	effective solder joint height
h(t)	hazard rate
$h_{SJ}(t)$	hazard rate of solder joints
$h_{SJB}(t)$	base hazard rate of solder joints
K_D	diagonal flexural strength
l, L	length
L_D	maximum distance between component solder joints
M	number of interconnections
n	empirical constant of the Coffin-Manson relation
n_c	number of components
N	number of thermal cycles
N_f	amount of cycles to failure
n_p	number of products
O	number of needed interconnections to maintain component functionality
Q	quad, or quad interconnection configuration
r	radius
R, R(t)	reliability, probabilistic reliability in given time
$R_{component}$	component intrinsic reliability
$R_{interconnection}$	interconnection reliability of component

S	substrate
T	temperature
t_D	half cycle dwell time
T_g	glass transition temperature
T_{SJ}	mean cyclic solder joint temperature
w	maximum warpage of component
W	width
x	fraction of failed items
α_1	coefficient of thermal expansion below glass transition temperature
α_2	coefficient of thermal expansion above glass transition temperature
α_c	coefficient of thermal expansion of component
α_{PWB}	coefficient of thermal expansion of Printed Wiring Board
α_s	coefficient of thermal expansion of substrate
β	Weibull shape parameter
ΔA	difference in solder land area
ΔD	cyclic fatigue damage
ΔT	temperature difference
ΔT_c	temperature difference in component level
ΔT_e	equivalent cycling temperature swing
ΔT_s	temperature difference in substrate level
$\Delta\alpha$	difference in thermal expansion of two materials
$\Delta\varepsilon_p$	plastic strain range during one cycle
ε	strain
ε'_f	fatigue ductility coefficient
η	Weibull characteristic life, at which 63.2% of population have failed
η_0	Weibull characteristic life in reference test
$\eta_{0,f}$	Weibull characteristic life in reference field conditions
λ	constant hazard rate of exponential distribution
λ_B	base hazard rate
λ_{SJ}	hazard rate of the solder joint
λ_{SJB}	base Hazard rate of the solder joints
μ	degree of angle
π_E	environmental stress factor
π_D	design stress factor
π_{SJDT}	failure rate multiplier

ASIC	Application Specific Integrated Circuit
A42	Alloy-42, Ni42Fe alloy
BGA	Ball Grid Array
BOM	Bill of Material
BT	Bismaleimide Triazine
CALCE	Center for Advanced Life Cycle Engineer, University of Maryland
CAM	Computer Aided Method
CD	Compact Disc
cdf	cumulative distribution function
CLLCC	Ceramic Leadless Chip Carrier
CPD	Cycles Per Day
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
DNP	Distance to Neutral Point
DOE	Design of Experiments
EU	European Union
FEM	Finite Element Modeling
FIT	Failures in Time, number of failures in 10^9 hours
FR-4	“Flame-Retardant”-4, commonly used PWB laminate
HDPUG	High Density Package User Group
IC	Integrated Circuit
i-FIT	Interconnection Failures In Time
JEDEC	Joint Electron Device Engineering Council
IPC	Institute of Interconnecting and Packaging Electronic Circuits
LLP	Leadless Package
μBGA	Micro Ball Grid Array
MC	Mold Compound
MH-217	Military Handbook 217
MTBF	Mean Time Between Failures
MTTF	Mean Time To Failure = 1/FIT
MTTR	Mean Time To Repair
NTC-C	Number of Thermal Cycle requirement C by IPC-9701
PC	Personal Computer
PBGA	Plastic Ball Grid Array
POF	Physics of Failure
PWB	Printed Wiring Board
QFN	Quad Flat No-lead package

RIAC	Reliability Information Analysis Center
RoHS	Restriction of Hazardous Substances, Directive by European Union
SMT	Surface Mount Technology
SPC	Standard Product Cost
TC	Thermal Cycle or number of thermal cycles
THT	Through Hole Technology
TSOP	Thin Small Outline Package
TSSOP	Thin Shrink Small Outline Package

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1 Introduction

The ever-increasing integration of electronics is setting high demands for the components, component packaging and their interconnections. To achieve the required level of integration, new packaging concepts and technologies are constantly introduced. Also, the average solder joint volume of the component interconnections has decreased during the last two decades. Moreover, the stress environments experienced by the components and their interconnections has at least remained the same. This sets a high demand for the stress resistance of the diminishing solder joints. Due to this, among other factors, the board level reliability test performance of the components has decreased gradually. This indicates also an increase on the component hazard rates due to the inadequate solder joint reliability. Furthermore, the risk that the interconnection hazard rates would bypass the component intrinsic hazard rates in the near future will get higher. To conclude, there is a need for hazard rate estimates of the component interconnections in different stress environments.

The technology selection is strongly driven by electrical performance and cost. Most of the packaging technologies are implemented first in the consumer electronics. Later on when a certain maturity level of a particular packaging technology is reached, it is implemented to infrastructure products. Moreover, the economical reasons drive the technology selections, as higher volumes decreases the average component costs.

The electrical performance of the components is continuously improving, following Moore's law (Moore 1965), which predicts that the number of transistors on an integrated circuit is increasing exponentially. To ensure the reliability of rapidly developing technologies, a deeper reliability analysis with sophisticated tools are needed. However, the results of the laboratory analysis are seldom used on the product life time predictions. The implementation of a new component or an interconnection technology introduces also a risk for product failures. Usually the amount of risk is unknown until enough reliability test data or field experience is gathered. In the worst case the risk analysis is totally ignored, which can lead to catastrophic product failures. This is due to, for example, a lack of in-house competence on component packaging technologies or with solder joint reliability management.

Component manufacturers are readily producing thermal cycling data of the component solder joints. Nonetheless, the presented data does not cover all the critical parameters, which are needed for an accurate design level life time

prediction. Furthermore, in the product development phase very accurate predictions can not be made due to the fact that the stresses induced to the product vary. This means that the product level predictions can not accurately be made on the individual product level. A lot of data of different electronic components packaging is available, but there does not exist a common understanding of how this data should be presented or further processed for the electronic product development needs.

The reliability management of an electronic product is a complex task. The product can be divided into an extreme amount of sub-parts, whose failure mechanisms are either systematic or random in their nature. One of these product sub-parts are the second level interconnections, namely the solder joints between the electronic component and the Printed Wiring Board (PWB). To manage the component solder joint initiated failures, the technology selections should be based on risk analysis. The solder joint hazard rate analysis should contain the thermal cycling results, the effects of the design and the environment. The result of all these should be presented in an understandable format. Usually the analyses contain only thermal cycling data, which is typically found to be of limited usage in product failure predictions. Without taking the aforementioned qualities into consideration, an interpretation of the test results to field failure expectations would result in very inaccurate predictions. This is due to the fact that the test and the end product systems are typically far too dissimilar.

Main aging mechanism for the infrastructure electronics is based on the daily thermal fluctuations, usually referred to as thermal cycling. As a result of thermal cycling the solder joints are stressed due to the different thermal expansions of the component and the PWB. The mechanical properties of the solder joint will degrade in time due to the changes at a microscopic level. Eventually the solder joint will rupture, as a result of a fatigue of the solder joints. The aging of the solder joints can be accelerated with dedicated thermal cycling tests, which help to determine the hazard rate of the component solder joints.

In the era of mature SnPb Through Hole Technology (THT) and early Surface Mount Technology (SMT) at the beginning of the 1990'ies, an usual accelerated thermal cycling test result for the characteristic life of component interconnections was at a level of 104 thermal cycles (Syed 1999). The level of hazard rate of such components is close to the Failures-In-Time (FIT) figures used in the earlier solder joint failure assessment methods, when a FIT figure of approximately 1 was used for solder joints (RIAC 2006). The current knowledge of the reliability behaviour of component interconnections is still heavily relying

on the data gathered from the early 1990 products. The board level interconnection tests made after the year 2000 show degradation in the thermal cycle test performance. Tests made for ceramic leadless components resulted in 800 to 900 thermal cycles for the Weibull characteristic life (Särkkä, Tammenmaa, Salmela & Andersson 2004). So, the achieved failure free time or the time to acceptable amount of failures has decreased in reliability testing to roughly 10–20% of the standard components of early 1990'ies. In spite of the fact that the methodology and the data has not been reassessed, a technological revolution of components and interconnection media has taken a place in SMT. This means in practise that the interconnection reliability predictions could be out of date. Furthermore, there is a tendency that solder joint failures will become dominant with the near future products, at least in very demanding usage environments. Within these frames, there is a clear need for a method for predicting the field hazard rates of solder joints.

1.1 The purpose of the thesis

The purpose of this thesis is to introduce tools and methods for a product level interconnection reliability analysis. The fundamental idea of the subject was evolved during the seven years in component packaging and interconnection technology evaluation and development work in Nokia Networks, followed in Nokia Siemens Networks. The component packaging qualifications are done under numerous quality instructions and due to that the results are proven to be reproducible. Meanwhile there was a lack of a practical way of utilizing this data into field risk analysis. This was emphasized when the Restriction of Hazardous Substances (RoHS) directive (EU 2003) was implemented on the 1st of July 2006 and the soldering material had to be changed. So, there was no field failure data available. As is said, the best innovations are based on a real need; this is just the analogy behind the method described in this research.

This thesis emphasizes the solder joint field failure estimates of surface mount components. In the thesis a novel method for converting the component qualification test data into field failure estimates is introduced. The method also takes into account the different stress levels due to the product design and the environment, which has not been made before for solder joints to such an extent. The method results in an accurate hazard rate prediction of component interconnections. Furthermore, novel component qualification criteria are introduced. Instead of using a generic qualification criterion for all of the different

component packaging technologies, component packaging specific criteria should be used. These criteria are intended to describe true failure behaviour of the component interconnections in the actual operational conditions. The benefit of such a method is to be able to estimate the suitability of a particular component in the given stress conditions and to avoid over-specification or over-designing.

There are numerous technical studies and research that include thermal cycling data, which is currently of no use for field failure estimates. The method described in this thesis utilizes the aforementioned data, and is the first published practical method to be used in the product field failure estimates. The method is based on scientific research and analysis, and can be easily further developed when field failure data is available.

A novel analysis method of interconnection failure costs is also presented. Such analysis, where interconnection elements are dealt as cost elements, has not been reported earlier according to the best knowledge of author. The main idea is to give a cost for the interconnection failures, which enables comparison of the different component packages to each other in respect of the life time costs.

Furthermore, the thesis introduces a novel production failure mechanism for Plastic Ball Grid Arrays (PBGA) and an estimation method for simulating the effect of bi-material incompatibility in a lead-free reflow. A variation analysis of the design and the process was also done in order to estimate their effect on the field reliability of the solder joints.

The purpose of this thesis is to present which tools and methods are needed for true component interconnection reliability analysis in the different usage conditions. Furthermore, the idea is to wide the component qualification criteria from simple accelerated stress test results to a true interconnection reliability analysis.

2 Overview of the second level interconnection reliability

In this Chapter the reliability concept is overviewed. It is shown that there are many definitions for the term reliability, and that reliability engineering is a concept with a lot of uncertainties. Also, the theory of the second level interconnection reliability is presented. In this thesis component interconnections refer to solder joints and the mechanical joints are excluded. Furthermore, the failure mechanisms of the solder joints under the applied stress and their effect on the product level are presented.

2.1 Reliability – overview and definitions

The utilization of the reliability concept in an engineering community is still to be further developed. There are many good theories in place, and some practical methods have been introduced. However, there is no unified community to develop total reliability concepts for the whole product life-cycle. For instance, there are many quality and reliability specifications and standards for the component manufacturers. In spite of that, even fulfilling all of those specifications and standards the reliability expectations are not met in the end-product level. This is due to the fact that the standards can not take the end product stress conditions into consideration.

Many scientific researches and industry studies concerning the board level reliability performance of particular components concentrate on analysing the results of the accelerated stress test. This data is useful in characterization of a new technology in the particular stress test. Also, the standardized accelerated stress tests (*e.g.* IPC-9701 2002) help the comparison of different technologies to each other. But, the aforementioned researches do not usually present the information in such form that it could be used in a product level failure occurrence prediction. So, in such studies the unreliability analysis applies only for particular designs and components in the given conditions. Furthermore, the thermal cycling data, meaning the failure occurrences during the tests, is commonly denoted as reliability analysis. To be accurate, this approach is not true, as the cumulative failures are related to the unreliability F by the reliability theory, where reliability R is given in specified conditions as $R = 1 – F$. As conclusion thermal cycling data is just one sub-phase of a true reliability analysis.

Fundamentally, the theory of electronics is based on the very well known and accurate, even complex, theories of electricity. There are powerful and user-friendly methods and tools based on the theories of electricity. One can predict very accurately the characteristics of an electronic circuit, when the components and their interconnections are known. To compare the electrical theories, methods and tools to the counterparts in the reliability area, one can make the conclusion that there are very many similarities between them. Nonetheless, the greatest difference between the electronics and the reliability theory is the lack of accurate measurement data and verification of the reliability predictions. In order to measure and collect such data, more efforts in the area of product field failure root cause analysis should be made due to the fact that the cause of failures has not been recorded accurately in the past. When there is no accurate data available, the verification of the reliability predictions can not be made. There is great potential for product reliability, if the electronics design tools would also include the reliability aspects.

From a historical point of view, the theories behind reliability analysis were developed as early as 1773 by Pierre-Simon Laplace (Rueda & Pawlak 2004). The reliability concept was evolved in the 1940'ies, in a very early stage of the modern electronics era. Due to some very unreliable components in the military electronics there was a need for 1) better field reliability data 2) higher quality components, 3) quantitative reliability requirements, 4) verifying tests prior to mass production and 5) standardization of the reliability discipline (Denson 1998). Items 1) and 2) are still on the top of the wish list of many reliability engineers in the electronics industry even today. In item 5) the emphasis was in the identification of root causes and the determination of mitigation actions (Denson 1998).

The reliability theory was started to be treated as a separate subject in the year 1961, by the paper published on coherent structures (Barlow 2002). The standard named MIL-HDBK-217 (MH-217) was introduced by the US Navy in 1962. This standard was used as a basis of the reliability predictions and it was constantly updated and developed to fulfil the requirements of the evolving electronics innovations. MH-217 had a focus on the physics of failure (POF) or models based on empirical data. The last version of MH-217 was published in 1992 and its empirical data based prediction models are maintained by the Reliability Information Analysis Centre (RIAC) to this day. Currently, the computer aided Finite Element Modelling (FEM) methods are far more popular than the prediction methods based on the empirical or semi-empirical models. The

most important reasons for this are the lack of accurate field reliability data and the easy-of-use tools of FEM. However, both of them have their own advantages and disadvantages.

The term *Reliability* is generally used to describe the long term performance of the products. In fact, it is a word with very many meanings and it is usually left undefined, as there was a common understanding and a clear definition for the term *Reliability.* Table 1 shows different definitions and interpretations of the term *Reliability.* Table 1 shows only few examples of the usage of the term and it is not completely studied in this thesis as the etymology or terminology was not an objective of the research. However, Table 1 gives an idea that the world of reliability is engineering with uncertainties, starting from the term itself. In the standard language, the term *Reliability* is often used as a synonym for *Quality*. The term *Quality* could be defined as a variation in the particular properties within a population of the subject, whereas *Reliability* is more related to the probability of the life-time expectancy of the population.

From a product designer and manufacturer point of view the expected reliability of a product is somewhat well known. However, the reliability expectations of the product vendors and the end-customers may be different. For instance, commonly accepted version of the definition of the *reliability* is as follows (MIL-STD-721C 1981),

> *"Reliability is the probability that a component, a sub-system or a system operating under stated conditions will survive for a stated period of time".*

From the end-customer point of view the stated *period of time* does vary from customer to customer. Also, the *under stated conditions* -part will be varying by many variables, *e.g.* geographical location, the awareness of the customer about the product usage specifications and by the end-user habitats, and so on. From an individual end-user point of view, the product is considered to be reliable, if the product has maintained its function for the time expected by the end-user himself. Furthermore, the customer is not willing to hear that there is a probability that the product will fail, like it could be interpreted from the common definition above.

So, the reliability is purely related to engineering philosophies. With sophisticated tools and with competent engineers, the reliability engineering is a solid part of a high quality product design starting from the beginning of the product design. Furthermore, a reliability prediction can be used to compare similar designs, for example, or it can be used to calculate spares needs and expected repair costs when in the field. Moreover, as the reliability can also be

denoted as a long term time-dimensional quality, the so called end-to-end quality thinking is reliability work in its purest nature. Nowadays, the greatest challenge of the reliability predictions and the reliability engineering is to keep going with the ever increasing pace of introducing new electronics technology innovations together with the lack of reliability data from the field.

Table 1. Different definitions and views of the term reliability and its theory. In this thesis the definition by O'Connor has been used.

Reference	Definition or interpretation of term Reliability
O'Connor 1999	"Reliability is the probability that an item will perform a required function without failure under stated conditions for a stated period of time"
IEEE 2007	"Reliability is a design engineering discipline which applies scientific knowledge to assure a product will perform its intended function for the required duration within a given environment."
Gavrilov 2006	"Reliability theory helps to clarify the difference between age (the passage of time) and aging (deterioration with age)"
General reliability theory	"Since reliability is a probability, it is a number between zero and one"
Tammenmaa 2007	"Reliability can be considered as a long term quality in the use conditions, *i.e.* as environment stress dependent, time dimensional quality" "Due to its character, any unambiguous value can't be given to reliability without accurately specified stress conditions"
Asia Market Research 2007	"Reliability refers to the extent that a measure of a concept would deliver the exact same results no matter how many times it is applied to random members of the same target group."
Online etymology dictionary 2007	1569, raliabill, from rely + -able. Not common before 1850 Rely, sense of "depend, trust" is from 1574 -ability, suffix expressing ability or capacity

2.2 Theory of interconnection reliability

In this Section interconnection reliability theories are introduced. The general reliability theories are utilized for this. Fig. 1 shows different approaches to component reliability, where the component intrinsic and its second level elements are shown. *Approach 1* is the most often used approach, where only the component intrinsic failures are taken into account. These failures include the failures at an IC level as well as at a component packaging level.

Approach 1 does not cover the failures caused by second level interconnections, namely the solder joints or mechanically pressed joints. This

approach is relevant for components with robust interconnections. In such systems the reliability of a component, R, is written simply as

$$R = R_{component}, \tag{1}$$

where $R_{component}$ is an intrinsic reliability of the component. *Approach 2* also takes into account the reliability of the second level interconnections. This approach is applicable for components whose second level interconnections are one of the main failure sources. The reliability equation for a component is then written

$$R = R_{component} \times R_{interconnection}, \tag{2}$$

where $R_{interconnection}$ is the reliability of the second level interconnections of the component. *Approach 3* is based on *approach 2*, but a redundancy of the interconnection elements is shown in detail. This is usually the case with many current component technologies, *e.g.* processors, where the supply voltage and ground is divided into many sub-nets. This is done to ensure the thermal and the electrical stability of a component. In spite of that, the most important interconnections, the signal inputs and outputs, do not usually have redundancy. The reliability function of a non-redundant interconnection element of *approach 3* is written

$$R_{interconnection} = \prod_{i=1}^{M} \left(R_{i,interconnection} \right), \tag{3}$$

where M is the number of the interconnections, $R_{i,interconnection}$ is a reliability of particular non-redundant interconnection element. The redundant part of *approach 3*, where the interconnection elements are in parallel, can mathematically be described as

$$R_{interconnection} = 1 - \prod_{i=1}^{M} \left(1 - R_{i,redundant\ interconnection} \right), \tag{4}$$

where M is the amount of parallel interconnection and $R_{i,redundant\ interconnection}$ is the reliability of each redundant interconnection element.

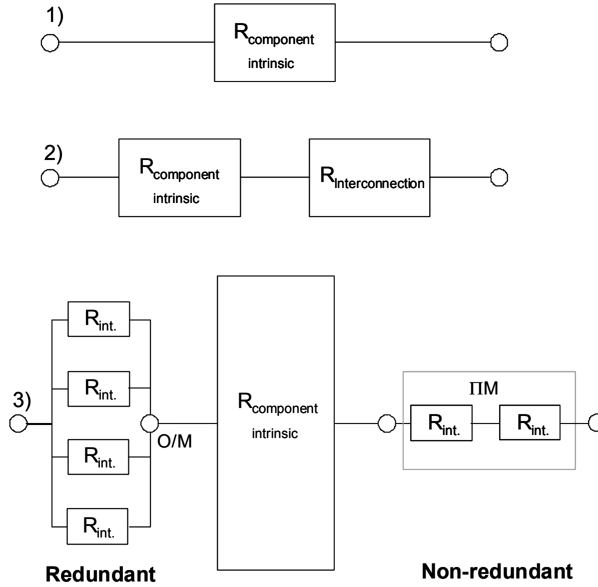

Fig. 1. A diagram representation of different approaches (*1–3*) of component reliability, divided to component intrinsic ($R_{component\ intrinsic}$) and its second level interconnection elements ($R_{int.}$). *O* and *M* denote to the amount of elements to work in order to maintain the functionality of the system.

In the redundant solder joint system there are multiple joints which have the same function in the system in order to improve the long term stability and reliability of the system. In such systems there is M pieces of interconnections of which a fraction of interconnections, denoted as O, must work to maintain the function of the system. This is referred to as an M-modular redundant system, which can mathematically be described as

$$R_{O/M} = 1 - \sum_{i=0}^{O-1} \left(\frac{M!}{(M-i)!i!} \right) R^{i}_{\text{interconnection}} \left(1 - R_{\text{interconnection}}\right)^{M-i}, \tag{5}$$

where $R_{interconnection}$ is the reliability of each interconnection element (O'Connor 1999). In practise every solder joint has its individual failure expectation, which would make the reliability calculation very complex in the M-modules redundant systems. In spite of that, the Equation 5 gives more realistic reliability expectations for redundant systems than the conservative reliability equations for interconnection elements. Fig. 2 shows the reliability of a redundant system as a function of reliability of each interconnection element, by using the Equation 5.

There are 10 solder joints in parallel. To achieve 90% reliability in the solder joint system, when two out of the ten solder joints must work to maintain the function of whole system, the reliability of one solder joint should be at least 34%. With the eight out of ten-scenario, the reliability of each solder joint should be at least 88%. As a reference, when ten solder joints are in series with respect to the reliability, a 98.95% reliability of each solder joint would be needed for 90% overall reliability.

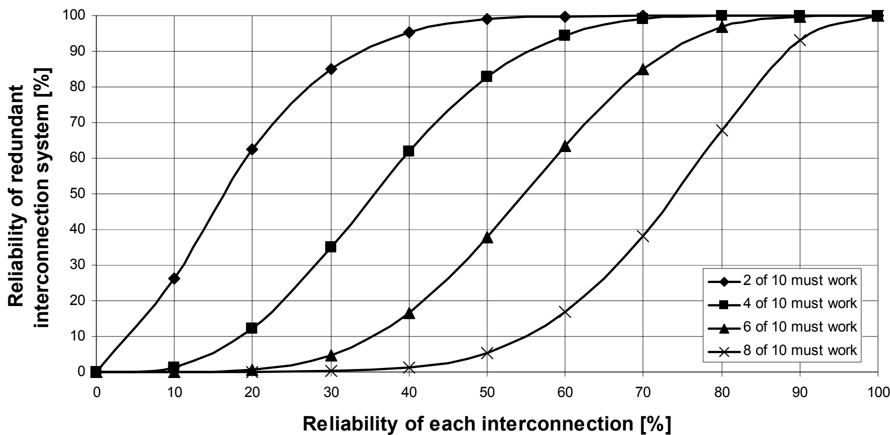

Fig. 2. Reliability of a redundant interconnection system as a function of the reliability of the interconnection elements. The interconnection system has 10 interconnection elements in parallel, of which a fraction must work in order to maintain the function of the whole system. 2/10, 4/10, 6/10 and 8/10 fractions are shown.

2.3 The levels of interconnections

There are numerous failure mechanisms involved in electronic systems, which can be roughly divided into hardware and software related failures and failure mechanisms. The hardware failure mechanisms are numerous, where one of the most common hardware failure mechanisms is related to component failure. Furthermore, the component failures could be divided into component intrinsic and component interconnection (extrinsic) failures. The component intrinsic failure mechanisms are not discussed in this thesis and the emphasis is on the interconnection failures.

Electronic systems are made of different level of components or sub-assemblies and their connections to each other (Brown 1998). The amount of connections reduces when getting closer to system level, Table 2. A closer look would result in ~10^{10} sub-elements and interconnections within a typical digital electronics. In practise it would be impossible to accurately predict the reliability of such system in every packaging and interconnection hierarchy level. Despite that, the total reliability concept should consist of every reliability element of the system. In this thesis the emphasis is on the second level interconnections, and in more detail in the solder joints. Non-soldering interconnection methods are excluded.

The typical solder joint count in a digital electronics board is between 10^4 and 10^5, Table 2. Failure in any of the solder joints will degrade the functionality of the product or in the worst case stop its function entirely. So, there are up to 10^5 failing elements in the digital product, which are usually left out of the risk analyses. In the most straightforward designs, where no redundancy is used, the failure in any of the components or their connections will lead instantly to system failure. In the current electronic devices, this vulnerability has been taken into account and enough redundancy has been applied in order to maintain the product function at least for the designed lifetime.

Table 2. Packaging and interconnection hierarchy and examples.

Level	Description *	Example	Amount
0	Gate to gate	Transistors in ASIC chip	2×10^9 **
1st	Chip to substrate	ASIC component	4400 ***
2nd	PWB level connections	Digital electronics	$10^4 < 10^5$ **
3rd	Connections between PWBs	Digital terminals	3200 ***
4th	Connections between sub-assemblies (rack tray)	Digital electronics	$10^2 < 10^3$ ***
5th	Connections between physically separate systems	Digital electronics	$< 10^2$ **

* Brown 1998, ** iNEMI 2004 & *** estimated by author

Interconnection reliability analysis has not been a solid part of the product reliability concept. This is mainly due to the interconnection technologies and the set of components used in the through hole and early surface mount technology era. On that time, mainly in 1970'ies to 1990'ies, the interconnection failures were not the main cause of the product failures. This can be verified from the MIL-HDBK-217F (1991), where the empirical data based solder joint base hazard

rates are given by 41 failures per 10^{12} hours for through hole assemblies and 69 failures per 10^{12} hours for reflow solder joints. To put this in perspective, the hazard rates are roughly a thousand times lower than the typical component intrinsic failures for current processors (*e.g.* Freescale 1999). This is due to the stress relieving leads together with relative high volume of solder and wide contact areas between lead and solder.

With the emphasis of miniaturization of the products, the components and their interconnections are getting smaller (Kivilahti 2002). This will lead inevitably to a situation where the interconnection failures will be playing a more significant role in product failures. New technologies are evolving continuously and the product design time is getting shorter. Furthermore, new technologies that do not have field experience are taken in to the new product designs with accelerating pace. New technology implementation will usually mean an advantage in respect of the competitors and value adding to the customers. In order to gain the trust to the new technology, powerful and user-friendly applications for failure estimates must be taken into use. Ignoring the importance of the second level interconnections would potentially result in catastrophic field performance at least in the very harsh usage environments and with so called long-life high reliability electronics.

The standard surface mount components, which are being manufactured under standardized and mature process steps, have been in use for over than two decades. Despite the long experience of these components, their solder joint reliability performance in the product field conditions has not been monitored under any specified or standardized procedure. With the ever increasing overall requirements for the electronics, the standard components may also become very risky. This development increases the need for a total reliability concept, where the interconnection elements are taken into account. This is emphasized with the higher risk component packages.

2.4 Stresses experienced by solder joints and the related failure mechanisms

In order to prevent product failures during its designed lifetime, the stresses experienced by the product should not exceed the strength of the product. Typical stresses experienced by materials are categorized as mechanical, thermal, electrical, radiation and chemical (Dasgupta & Pecht 1991). From these stress types, only the radiation stresses are not relevant from the solder joint system

point of view. The typical stress levels experienced by the products are somewhat well known and the products are tested against them in the product development phase. Moreover, there can be a variation in the stress and strength levels of individual products, due to the stress and strength variation in the sub-parts of the product. As a result of the variation in the stress and the strength, there is a probability that the stress level exceeds the strength of the individual product. Fig. 3 illustrates an example of the strength and stress distributions in a product population. Theoretically, the failures can occur in the overlapping area of the two curves. In practise the strength of the product will gradually degrade under the stress and the strength curvature in the Fig. 3 will shift to the left. This is a new presentation of the aging effect on the strength characteristics of product population. Shear force measurements for power cycled SnAgCu soldered 1206 resistors showed a gradual degradation of shear force down to 10% of the original level (Stam & Davitt 2001). The degradation of material mechanical properties in time is referred to as aging. Due to aging the overlapping area of the stress and strength curves will increase and the probability of the product failure also increases.

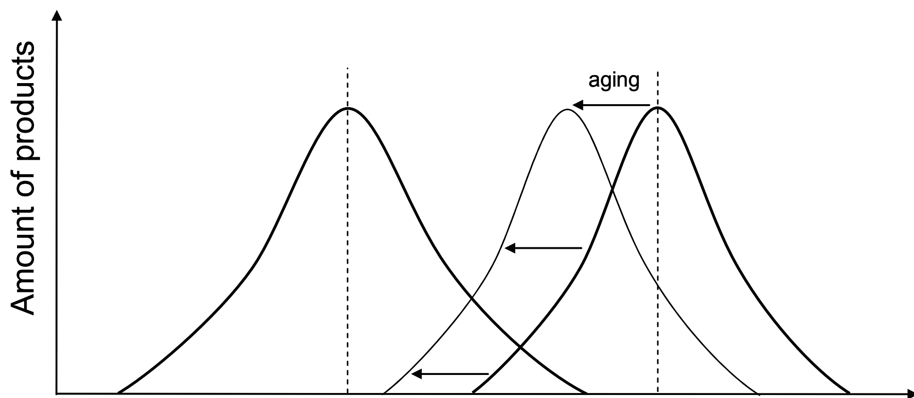

Fig. 3. Stress-strength distribution of a product population. The overlapping part describes the probability for the product failures. The strength of the product will gradually degrade (aging).

Fig. 4 shows a typical approach to product total failure estimates in time, with constant component hazard rate. The failures are based on randomly failed individual products that could be a result of quality variation within the product population. It gives somewhat adequate estimates of product failures, especially

when the product component set is based on mature technology, the usage environment will be quite the same and the stress levels do not exceed the strength of the product. In order to make reasonable credible predictions, the new system must be similar to well known existing system without involving significant technological risks (O'Connor 1999).

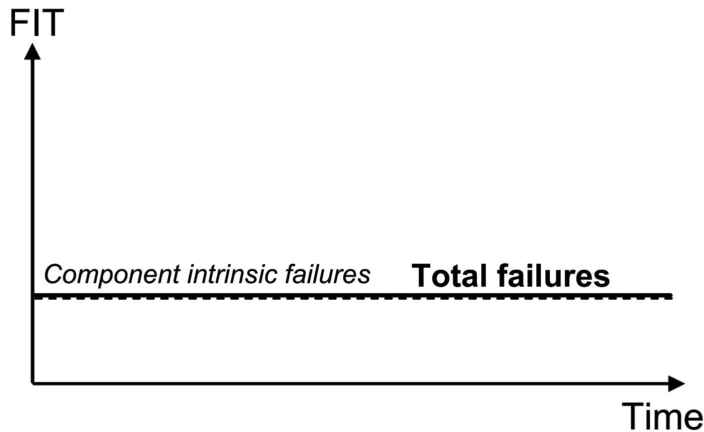

Fig. 4. Product failures-in-time (FIT) caused by components with constant hazard rate.

However, if any of the components hazard rates starts to increase during the design lifetime of the product, the constant hazard rate approach is not relevant anymore. In practise the total hazard rate is a sum of a time-independent constant hazard rate and a time-dependent increasing hazard rate with infant mortality region included. So, the product hazard rate would look more like the so called bathtub curve shown in Fig. 5. The component intrinsic failures will increase in time, which will increase the hazard rate. If the total product hazard rate is presented, the other failure modes, *e.g.* the interconnection failures, should be included. This addition increases the hazard rate even further.

In the literature, there are numerous studies concerning the solder joint failure mechanisms (*e.g.* Dasgupta & Pecht 1991, Clech, Manock, Noctor, Bader & Augis 1993, Wassink 1994, Engelmaier 1997 and Dunford, Canumalla & Viswanadham 2004). The solder joint failure (solder crack) is fundamentally a low-cycle fatigue, which follows the well known Coffin-Manson relation (Hwang 2001: 76). Low cycle fatigue is considered to be related to "plastic-strain fatigue" (Klesnil & Lukas 1980). However, three sources for solder cracking can be

distinguished, which are overload, long lasting permanent load and cyclic load (Wassink & Verguld 1995). The causes for the latter two are creep and fatigue, respectively (Wassink & Verguld 1995).

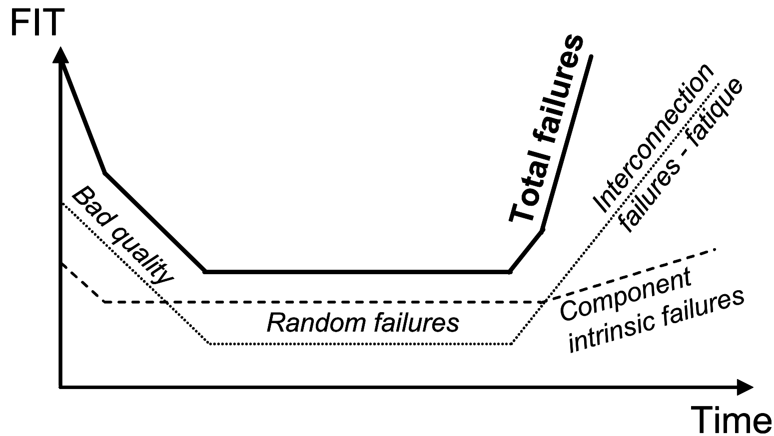

Fig. 5. Product failures-in-time (FIT) caused by component intrinsic and interconnection failures. Material and system aging mechanisms are involved.

Some estimates about the usage conditions and stress levels experienced by the components and their solder joints are published (*e.g.* Kiang 1998, Blish, Huber & Durrant 1999, HDPUG 1999, IPC-9701 2002 & JESD94 2004). In the references the stress conditions are divided into different device type and environment categories, which also describe general level requirements for the devices. The approach is in the product category level (IPC-SM-785 1992) and the stress variation of individual products is not taken into account.

In order to predict the solder joint failure occurrence under field conditions, the stress levels in the field must be known. Furthermore, an interpretation method to utilize the accelerated stress test data for failure prediction is needed. There have been some reported prediction methods for estimating the second level interconnection failures (*e.g.* Norris & Landzberg 1969, Engelmaier 1990 & Salmela, Andersson, Perttula, Särkkä & Tammenmaa 2006). These models are based on the empirical data and are relatively accurate. What is common to these prediction methods is that they have unfortunately not been taken into wider use in the product level reliability analysis. The aforementioned methods have a great deal of data and analysis behind them, but their usage has not found it's way to

the real Mean Time To Failures (MTTF) calculations as such, which means in practise that they are not a solid part of product development activities.

The fundamental idea behind accelerated stress testing is first to identify the stress conditions in the field environment. In the test phase the stress levels are then increased in order to accelerate the failure occurrence. Correctly chosen test parameters ensure the shortest test time and correct analysis, *e.g.* by using Design of Experiments (DOE) methods. This approach will result in improved reliability in product design. However, randomly selected test set-up usually leads only to wasting the research resources.

The failure definition is one of the key tasks in the accelerated stress tests. For example, the solder joint failure can be defined as an irreversible change in electrical resistance. For example IPC-9701 (2002) specifies that the joint has failed when 20% resistance increase has been detected with data logger within five consecutive scans. Usually when the first anomalies in the continuous monitoring data are detected, no macroscopic deformations can be observed. In spite of that, when looking deeper into the solder joint, the fundamental analysis would point the failure root cause to the deformations in the grain or grain boundary level, meaning that the solder material has aged. The next step, further inside the solder material, would go to the atomic level research. One could assume that atomic level research would give more answers about the aging characteristics of the solder. However, as is fundamentally known, the atoms do not age according to traditional physics. Thus it could be stated that the smallest aging elements in the solder joint system are the crystal lattices and their defects.

Another conclusion is that a failure can be indirectly detected by electrical measurements without going into the analysis, for instance, in the crystal level of material. By widening this idea, the properties of material can be divided in two categories, to so called intrinsic material properties and extrinsic material properties. The extrinsic properties are such macro level properties which can be directly or indirectly measured in the macro level. The intrinsic material properties are the foundation of the extrinsic properties and can not usually be directly measured. Some of the most important properties of a solder joint system, including some important metallurgical phenomena are presented in Table 3 (Hwang 2001: 65–69). From solder joint mechanical stability point of view, the stress-strain behaviour, the creep resistance and the fatigue resistance are the most important properties (Hwang 2001: 68).

The aging mechanisms of the solder joints depend on the stress conditions and the thermo-mechanical properties of the soldering system. The solder joint

material does have multiple properties that affect the failure occurrence. The aging of the solder takes place in the intrinsic material property level and it might not be detectable in macroscopic level before final material property degradation. The material aging models have been developed to estimate the failure occurrence in different stress conditions (*e.g.* Engelmaier 1997). To model the aging of solder, constitutive models of solder material have been developed, *e.g.* the constitutive models by Anand & Darveaux (Darveaux 2000) and Knecht & Fox (1990).

Table 3. Material properties and phenomena of a solder joint system (Hwang 2001: 65–69).

Property type	Examples of the properties
Physical	1. Phase-transition temperature
	2. Electrical conductivity
	3. Thermal conductivity
	4. Coefficient of thermal expansion
	5. Surface tension
Mechanical	1. Stress-strain behaviour
	2. Creep resistance
	3. Fatigue resistance
Metallurgical phenomena	1. Plastic deformation
	2. Strain-hardening
	3. Recovery process
	4. Recrystallization
	5. Solution hardening

Within the solder aging models the solder deformation rate, or the solder strain rate, is divided in sub-strain rates of elastic, viscoelastic, creep and plastic deformations (Dudek, Walter, Doering & Michel 2004). For low cyclic loadings of solder, with low temperature ramp rates, the creep is the most important part of strain, dominated by secondary, or steady-state, creep (Dudek *et al.* 2004). The strain rates in the secondary creep are close to constant, hence the name steady-state creep. Creep is the result of an applied static stress, in which the material relieves the stresses with plastic deformation (Hwang 2001: 68).

The plastic deformation is caused, among others, by the secondary creep, which is controlled *e.g.* by the movement of dislocations in the slip planes (Lindroos, Sulonen & Veistinen 1986). Creep in solder is due to dislocation climb mechanism or due to grain boundary sliding and by intergranular or transgranular void migration (grain boundary diffusion) (Dasgupta & Pecht 1990). Dunford *et*

al. (2004) published that most relevant creep deformation mechanisms with lead-free solders are dislocation creep, diffusion creep and grain boundary sliding. In recent years, many lead-free creep constitutive models have been developed (*e.g.* Wiese, Meusel & Wolter 2003, Schubert, Dudek, Auerswald, Gollhardt, Michel & Reichl 2003 and Dudek *et al.* 2004), which emphasizes the importance of understanding the creep mechanisms behind the solder joint failures.

When solder joints are subjected to cyclic stress environments, *e.g.* thermal cycling, the solder joints can fracture at stress levels below the yield strength (Hwang 2001: 68). This solder joint fatigue is based on a plastic deformation in the microscopic level, whereas it is not observed in the macroscopic level (*e.g.* Lindroos *et al.* 1986). The fatigue failure can be divided in to three phases: 1) crack nucleation 2) crack propagation and 3) final fracture (Lindroos *et al.* 1986:792). The crack nucleation is preceded by microstructural changes, *e.g.* local grain growth (Wassink 1994: 191). Examples of crack nucleation mechanisms are presented in Table 4 (Klesnil & Lukas 1980). The crack propagation starts with crystallographic propagation, which is followed by non-crystallographic propagation. The latter has a faster propagation rate and only one crack is usually propagating (Klesnil & Lukas 1980: 81).

Table 4. Mechanisms of crack nucleation (Klesnil & Lukas 1980).

#	Mechanism
1	Coarse slip on alternating parallel slip planes
2	Local brittle fracture
3	Condensation of vacancies
4	Loss of coherency across a slip plane due to accumulation of defects
5	Nucleation of cracks in grain boundaries

One mechanism behind the solder fatigue is the recrystallization followed by the grain growth, where the contaminants and microvoids coalesces in the grain boundaries and weakens the solder joint mechanical properties (Engelmaier 1997). The fracture can nucleate and propagate from the defects in the grain boundaries and eventually end as a full fracture (Engelmaier 1997). Coffin and Manson explained the fatigue crack growth in the terms of plastic strain (Manson 1953, Coffin 1954). This generally used relation for low cycle fatigue is expressed by

$$N\left(\Delta\varepsilon_p\right)^n = C_{pf}, \qquad (6)$$

where N is the number of cycles to failure, n is an empirical constant, $\Delta\varepsilon_p$ the plastic strain range during one cycle and C_{pf} is a proportionality factor (Norris & Landzberg 1969). By using Equation 6 the comparison between different strain ranges can be made. The Coffin-Manson relation has been accepted as a basis for many solder fatigue models. The Coffin-Manson relation is also the basis of so called Norris-Landzberg relation, which is utilized in this thesis and will be discussed in more detail in Section 5.2.3. The Norris-Landzberg relation was recently reviewed by Salmela (2007) and by Pan *et al.* (2005) to update it to correspond with the SnAgCu solder.

Examples of stress conditions and failure mechanisms experienced by solder joints are shown in Table 5. As stated, the creep and fatigue are the failure mechanisms for solder joint system, which are typical examples of wear-out failures of solder joints. On the other hand, brittle fractures are typical in the shock environments, *i.e.* high acceleration caused by drop. In order to accelerate the primary failure mechanisms of solder joints, thermal fatigue and creep, thermal cycling and vibration based tests are used. The thermal cycling, as a reliability test method, has been in wide use for decades. The vibration tests are usually done in the product verification phases, at least for the infrastructure electronics products. The shock and drop tests are commonly used for the devices, which might experience such stress conditions during their life-time. For example cellular phones are tested against the drop shock loadings. The products are also tested against the corrosive field environments, but the solder material itself is not typically the first to fail. So in the bottom line, the thermal cycling test performance as a measure of *reliability* has been accepted as a solid method to test the aging mechanisms of the solder joints.

Table 5. An example of stress conditions experienced by solder joints and the related failure mechanisms.

Failure mechanism	Stress environment	Description
Fatigue [*]	Cyclic stress, thermal [*] or vibration [***]	Fatigue failure initiates with micro crack and propagates to solder crack in cyclic stresses [***]
Creep [*]	Long-lasting permanent load [*]	Global plastic deformation of solder under static mechanical stress and temperature [**]
Corrosion [****]	Galvanic pair [****]	Metals with different electrochemical potential are in contact to cause material loss in the anode metal [****]
Brittle Fracture [*****]	Drop or shock [*****]	Fracture occurs in the brittle intermetallics layer of solder joint [*****]

[*] Wassink & Verguld 1995:83-85; [**] Hwang 2001:68; [***] Engelmaier 1997; [****] Vianco 1999; [*****] *e.g.* Mattila, Marjamäki & Kivilahti 2006 and Prabhu, Schaefer & Patil 2000

2.5 Effect of second level interconnection failure

Interconnection failures are observed at first as degradation in the product performance and will inevitable lead, after all, to product failure. This will happen if the redundancy was used in the design or not. Fig. 6 shows measured electrical resistance over four solder joints of one component in the accelerated stress test. One can note that after stable 450 hours in the test, there is approximately 100 h region, when the aging of the solder joint can be detected by the resistance measurements. This is due to solder joint crack which has started to propagate, Fig. 7. In this region, the product performance starts to degrade, and might cause short periods of product malfunction. If the product is sent to repair, a failure may not be detected at all (No Faults Found). Moreover, with the Radio Frequency/Microwave applications the degradation of the signal integrity can be detected with the S-parameter measurements as an increase in return loss in the crack propagation phase (Putaala, Kangasvieri, Nousiainen, Jantunen & Moilanen 2006). When the solder joint crack propagates further to full rupture, there will be two surfaces very close to each other in both sides of the solder joint rupture, Fig. 8. During the thermal fluctuations, the contact area of these two surfaces is continuously changing. As a result of this, the resistance over the joint will be unstable. This behaviour is also assisted with the surface contamination. After all, the product will fail as a result of the solder joint aging. In order to prevent the failures, the solder joints should stay in stable region with a certain safety limit.

RIAC (2006: 145-147) has collected failure causes of electronic systems. In the study, there is no particular category for the interconnection failures. This is

mostly due to the fact that the failures are not investigated, and only the initial symptom of the failure is recorded. The interconnection failures can usually be found under the *manufacturing*, *wearout* or *design* categories, but they can be a part of any other category (RIAC 2006: 145–147). This study is in line with other similar studies concerning the missing analysis of solder joint failures. As a conclusion, there is no accurate record of the solder joint failures. This results in the predictions relying predominantly on simulation methods.

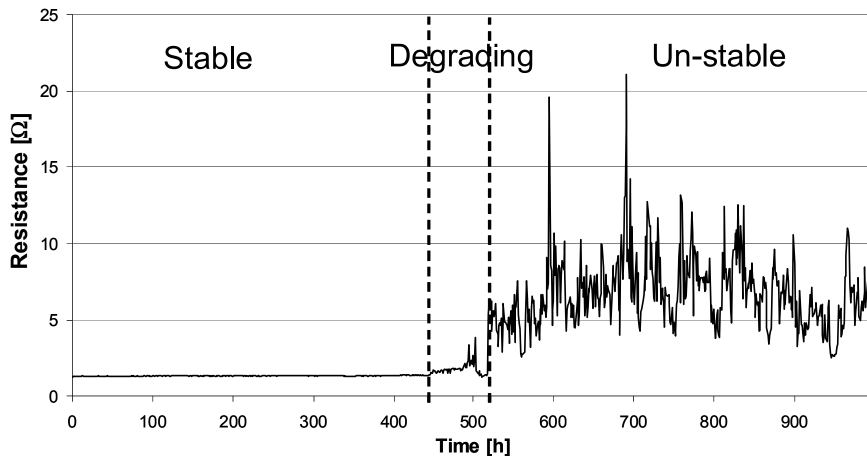

Fig. 6. Measured electrical resistance over four solder joints of a ceramic leadless component as a function of time in the accelerated stress test.

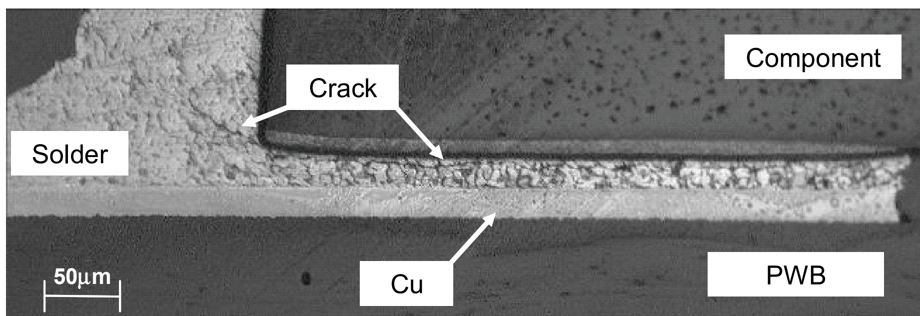

Fig. 7. Microsection of SnPb solder joint of a ceramic leadless component after accelerated stress test. Crack paths are already starting to propagate. The electrical and mechanical properties of the solder joint have degraded (refer to Fig. 6). Such solder joints might be seen as degraded product performance.

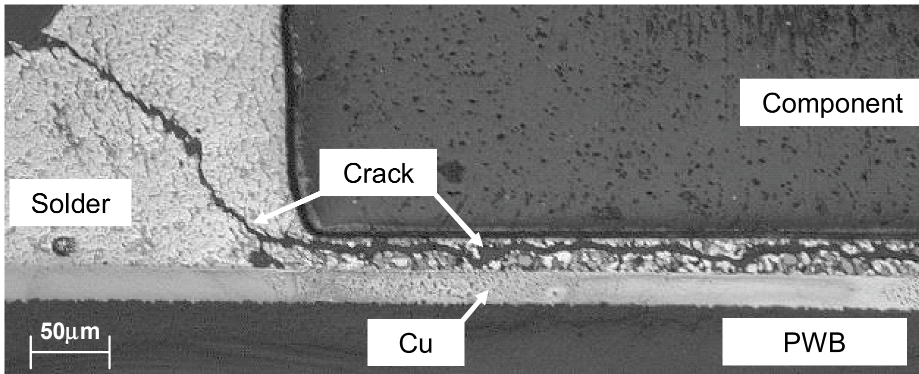

Fig. 8. Microsection of SnPb solder joint of a ceramic leadless component after accelerated stress test. The crack path has fully developed. The electrical and mechanical properties of the solder joint are totally gone, or at least they are very unstable (refer to Fig. 6). Note that the electrical and mechanical connect might still exist in some part of the solder joint; figure shows only two-dimensional microsection of the solder joint.

2.6 Standards related to solder joint reliability testing

As the thermal cycling has been accepted as a common component and board level reliability test method, there has been a need for standardization of the test methods. The Association Connecting Electronics Industries (denoted as IPC for its former name) has a wide selection of standards for the reliability test methods and requirements. Table 6 shows the IPC-specifications for the tests of board level interconnections. The IPC-9701 is a widely used reference in the electronics industry, even though it does not explicitly define the requirements for the thermal cycling test characteristics. Table 7 shows temperature cycling condition options specified by IPC 9701 (TC1-TC5). The test setup and result requirements of IPC-9701 are made for qualification purposes and the data is not currently used for field failure predictions. The IPC-9701 (2002) includes also new appendix for lead-free solders, which refers to recently published accelerations models for lead-free solders.

Table 6. Examples of specifications on component interconnection tests.

Standard	Description of the Standard
IPC-9701	Solder Joint Reliability – performance test methods and qualification requirements for surface mount solder attachment. For long term reliability or fatigue fallout
IPC-9702	Monotonic Bend Test – monotonic bend characterization of board level interconnects. For resistance to strain
IPC-9703	Mechanical Shock Test Methods and Qualification Requirements for Surface Mount Solder Attachments
IPC-D-279	Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

Table 7. Temperature cycling conditions per IPC9701 (2002).

Min. Temperature [°C]	Max. Temperature [°C]	Test condition
0	100	TC1
–25	100	TC2
–40	125	TC3
–55	125	TC4
–55	100	TC5

3 Solder joint reliability management

In this Chapter solder joint reliability management concepts are presented. The component packaging type specific reliability assessment method is introduced, which is presented in detail in Chapter 5. Also, a stress based reliability analysis method is presented, which helps to meet the product reliability goals when the stress environment is not accurately known.

During the product development certain processes and quality verifications are conducted in order to meet the requirements set to the product, *e.g.* certain level of functionality and reliability. At a certain phase the components are tested against *i.e.* the specifications of electrical functionality, manufacturability and reliability. In the component selection process there are three distinguishable component packaging verification concepts, which are 1) 0% test coverage 2) identifying and concentrating on the most critical technologies or 3) 100% test coverage. It is obvious that 3) requires huge amount of resources to execute and its cost-benefit might be questionable. Furthermore the 0% test coverage leads to unknown risks and the consequences might be catastrophic. In order to save resources the component package qualification data should be able to be used for the field hazard rate estimates. However, there is currently no practical method for utilizing such data and the current risk analyses are based on the past technology. A novel method to utilize the component package board level qualification data is presented in Section 3.2.

3.1 Backward and forward reliability

As the component and interconnection technologies are constantly developed and new evolving technologies are presented regularly, new possibilities and challenges are brought to industry. The technology development is driven by the increasing demands for the electronics, as well as the legislations, *e.g.* the Restriction of Hazardous Substances (RoHS) by European Union (EU 2003). The new technology is studied and characterized in the *fundamental research* phase (Fig. 9). This research is commonly done by universities together with commercial and independent research laboratories. From the solder joint technology point of view, the material characteristic and failure mechanisms related to new joining materials are revealed in this phase; being very important for the successful usage of new materials or technology. For instance, when new materials are taken into use without any history data of its real behavior in the

product usage environment, one is not able to predict neither the failure occurrence nor the root cause of the failure when they occur. So, in order to find the root cause of failure and a corrective action for it, the material is investigated by the means of *fundamental research*. After successful characterization, the commercial companies and the universities are investigating the benefits and possible implementation of the technology or material in the *Technology research* and *Technology implementation* phases. These phases gain knowledge of the technology in the short-run-production level and would help to reveal the main obstacles of the technology usage. Anyway, no field performance data is gathered in this phase. After the technology implementation, reliability data is gathered from the field experiences in the *Technology in use* phase. The data is mature enough when one production population has reached its end-of-life stage. So, in the infrastructure telecommunication area, it takes up to 7–20 years to completely rely on the field data of the technology. In this stage the data is mature enough to be used in the accurate field failure estimations. However, the technology might be obsolete at this stage.

In the area of electronics joining technologies, there is enough data available for pressfit connections and for SnPb assemblies excluding the latest component package development. Currently, the lead-free electronics is in the *technology in use* phase in the different electronics industry areas and first applications are already collecting the field data. Thus, the electronics industry must wait for some years to completely rely on the data gathered from the field.

In order to estimate hazard rate of an electronic device, two basic approaches can be taken. These approaches are dependent on whether there is real field experience available or a new technology or process is taken in to use. These two different concepts could be named as Backward Reliability and Forward Reliability, explained in Fig. 10. In the Backward Reliability concept, the cumulative past knowledge and experience are used for the reliability estimates of an electronic device. This is usually very effective and the estimates can be done with minimal resources. The only limitation is that the Bill of Material (BOM) and the processes used should not contain any major differences, unless the data and method is useless. The Forward Reliability concept utilizes accurate information, such as material properties and effects of different levels of stress, to estimate the reliability performance of an electronic device by modelling. The knowledge of the behaviour of the product in different stress levels from the product design phase is essential. Also an accurate estimation of the stress levels due to design and environment should be known. During the product life cycle,

the reliability estimates should be compared to the actual performance. This is essential for the model development and its accuracy.

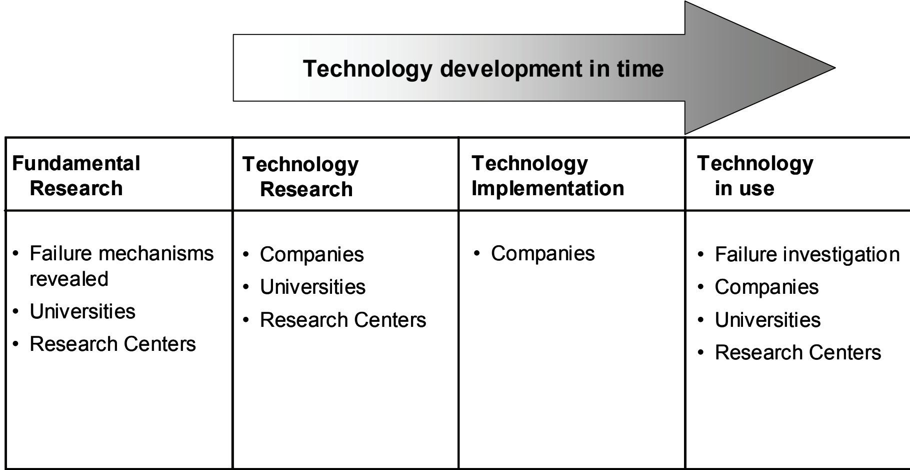

Fig. 9. An example of technology development in time and responsible parties.

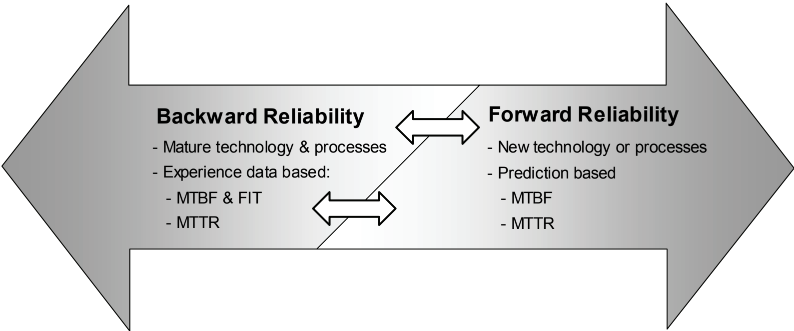

Fig. 10. A schematic presentation of Backward and Forward Reliability concepts. These concepts are not mutually exclusive, *e.g.* that the data from Backward Reliability can be used as an input for the Forward Reliability tools.

The Backward and Forward Reliability concepts are not mutually exclusive, so that the tools, methods and data can be used across both concepts. Table 8 shows the method description, notes, level of errors and the needed competence level for the basic and cross-linked concepts. For minor product changes and for component interconnections the Forward Reliability methods used with Backward Reliability figures approach should be used.

Table 8. Different approaches of the Backward and Forward Reliability concept.

	Backward Reliability	Forward Reliability
Method	Real experience from the field used for reliability estimates without modelling or analysis	Reliability estimates of new technology are purely based on modelling
Notes	Same technology and process used	Failure mechanisms and stress levels should accurately be known
Error level	Minimum to Moderate	Moderate to High
Competence level	Low	High

	Forward Reliability methods used in Backward Reliability	Backward Reliability data used in Forward Reliability estimates
Method	Real experience used for reliability estimates by using modelling and analysis tools	Using past technology experience to estimate new technology performance without analysis
Notes	Estimating the effects of minor changes or different environments. Used also for model development	Accuracy depends on the level of difference between technologies. Usually mis-used in industry
Error	Minimum	High to Infinite
Competence level	Medium to High	Very High

The usual source of high deviations, or errors, in the predicted and actual reliability performance, is the incorrectly chosen reliability prediction method. When the data from the past technology is used for the new technology predictions, the error could be large. This kind of method is more closely related to guessing than predicting. The prediction is fundamentally based on the knowledge of material behavior in the different stress conditions. In the material related aging predictions, there is an analogy with the traditional Newtonian physics, where the unknown parameter can accurately be calculated when knowing all the other parameters involved. The guessing instead is not based on any knowledge of physical property. In spite of that, so called educational guesses are used in the electronics industry, when there is no practical method of predicting the performance of the particular product in the not-well known stress environment. However, crosswise usage of both concepts utilizes a scientific approach, as it involves a theory of the performance, which is then measured and further developed.

3.1.1 Backward reliability concept

The Backward Reliability concept utilizes the experiences from the past products and tests. In this case, the technology is mature and the production phases have been established and the production quality level and yield are high. The technology has been completely characterized and the root causes of typical problems have been identified and their solutions have been proven to be in place. The gained knowledge can be used for the new product development as such, or with minor adjustments by the product design or its usage environment.

In the area of solder joint technologies, the components in the SnPb era are fully characterized and their root causes and solutions are well known. So, with the information of the stress levels in the product and its usage environment, lifetime expectancy and a failure occurrence can be estimated rather accurately.

An empirical or a semi-empirical models and methods for metal systems are being developed by *i.e.* Engelmaier (1993), Norris and Landzberg (1969), Iannuzzelli (1993), Clech *et al.* (1993) and Monkman & Grant (Hwang 2001: 76). They have investigated *e.g.* the SnPb solder in the past years. Recently, there have been updates for the aforementioned models, *e.g.* by Salmela *et al.* (2006), Dudek *et al.* (2004), Wiese *et al.*(2003) and Schubert *et al.* (2003).

The failure occurrences from the past technology have been recorded to failures-in-time figures (FIT). These are used in the Mean Time Between Failure (MTBF) calculations. MTBF quantifies the failures for repairable systems and is calculated by

$$MTBF = MTTF + MTTR, \tag{7}$$

where MTTF and MTTR are Mean Time To Failure and Mean Time To Repair, respectively. The MTTF is simply the reciprocal of the hazard rate and is written

$$MTTF = \frac{1}{\lambda}, \tag{8}$$

where λ is the hazard rate or the FIT figure (O’Connor 1999). Since usually MTBF >> MTTR, the MTBF can be approximated by

$$MTBF \cong MTTF = \frac{1}{\lambda}. \tag{9}$$

The MTBF gives adequate measures and is quite useful when different products or different field conditions are compared. But when operation hours are

cumulated for some years the MTBF is not very sensitive for the failures. The MTBF has a slow response to evolving hazard rates, and therefore it is not a tool for revealing the failure mechanisms caused by aging. The MTBF figure tends to saturate when large amount of products have gained enough time in field.

The MTBF is a very useful concept of describing the constant hazard rates. However the interconnection failures that occur during wear out, where the hazard rate is not constant, can not be described with MTBF.

3.1.2 Forward reliability concept

The Forward Reliability concept can be used when new technology or material is taken into use and there is no history data available of the life time performance. The effect of the new technology is assessed with accelerated tests or by simulating. The accelerated stress tests are speeding up the relevant failure mechanisms in order to estimate the reliability performance within the stress conditions in the field. The simulating models and empirical models have been developed to estimate the difference of the given stress environments and the behaviour of the component interconnections on those.

Different types of acceleration stress tests have been developed to estimate the failure occurrence of the product or component. These tests include thermal cycling, vibration, and shock loadings. The tests can be a qualification or material characteristics type of tests. The qualification test result is simply ‘passed or failed’, whereas the characteristic tests help to understand the material behaviour in more detail. This data can be used in the field failure estimates. The requirements for the qualification tests are based on the experiences from the field conditions.

The simulation models can be divided into computer aided and empirical models. Finite Element Method (FEM) is a Computer Aided Method (CAM) for numerical solution of field problems. The FEM is a powerful tool for assessing multi-geometrical shapes. With the solder joints, FEM is used to compare the different stress conditions to each other and the resulted acceleration factor is used for reliability expectations. Examples of commonly used interpretation methods for solders are by Anand (1985) and Darveaux (2000). The FEM makes possible to utilize the so called virtual prototyping, where design verification can be done in a shortened time.

The approach, where the Forward Reliability methods are used with Backward Reliability data can be used when minor changes or variation effects

are estimated. This approach fits also to the interconnection failure analysis, because the soldering material and the PWB are usually the same. Only the type of component has changed, and when its material properties and geometry are known, the failure estimations can be made accurately.

3.2 Packaging and interconnection category based reliability assessments

Packaging and interconnection category based assessment method is a novel method for estimating the interconnection failures in the given stress conditions. The method utilizes the thermal cycling data from the component manufacturers or other laboratory test data. This data is currently used only for qualification purposes; the following procedure presents how this data can be used for reliability estimating purposes in the product development.

Let us assume that similar component types perform similarly at the accelerated test and in the field conditions. Based on this assumption, the basic elements of an interconnection system would consist of four different groups interacting with each other. The groups are 1) the component 2) the solder joint, 3) the substrate and 4) the surrounding environment, as illustrated in Fig. 11. These elements interact in the lowest hardware levels, namely in the level of material properties. Usually, in the case of interconnection failure, the cause of fault is pointed to the component itself. This approach means that the investigator has taken the perspective of 2) the solder joint, 3) the substrate or 4) the environment. To investigate the interconnection failures or more precisely, the solder joint failures, one should take the perspective of the solder joint itself. This means that the cause of failure should be investigated from the lowest hardware levels of 1) the component, 3) the substrate or 4) the environment or any other combination of the aforementioned. This approach includes the fact that the element, from where the perspective has been taken, is purely non faulty. This generalization is seldom completely true in real interconnection systems, but is used as a basic assumption in this thesis.

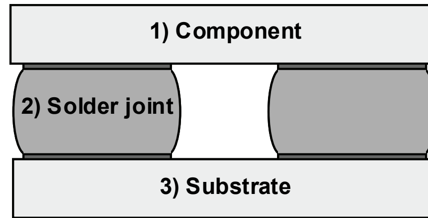

Fig. 11. The basic elements of a second level interconnection system.

In the component package category based assessments the analysis is started from the solder joint level, so, from the solder joint perspective. In the analysis, the component packages are categorized to finite amount of packaging classes. These packaging classes are dealt as blocks, which has only the measures of *component packaging type* and *normalized stress test result*. The latter is based on the accelerated stress test conditions and accelerated stress test result. When these figures are known, the analysis utilizes readily calculated multipliers for each basic interconnection element to estimate the field performance based on the stress difference analysis. Fig. 12 shows the process step for the component package category based analysis. This novel method is accurate and easy to use and is presented in detail in Chapter 5. A hazard rate estimation of the component interconnections in the given usage conditions is resulted.

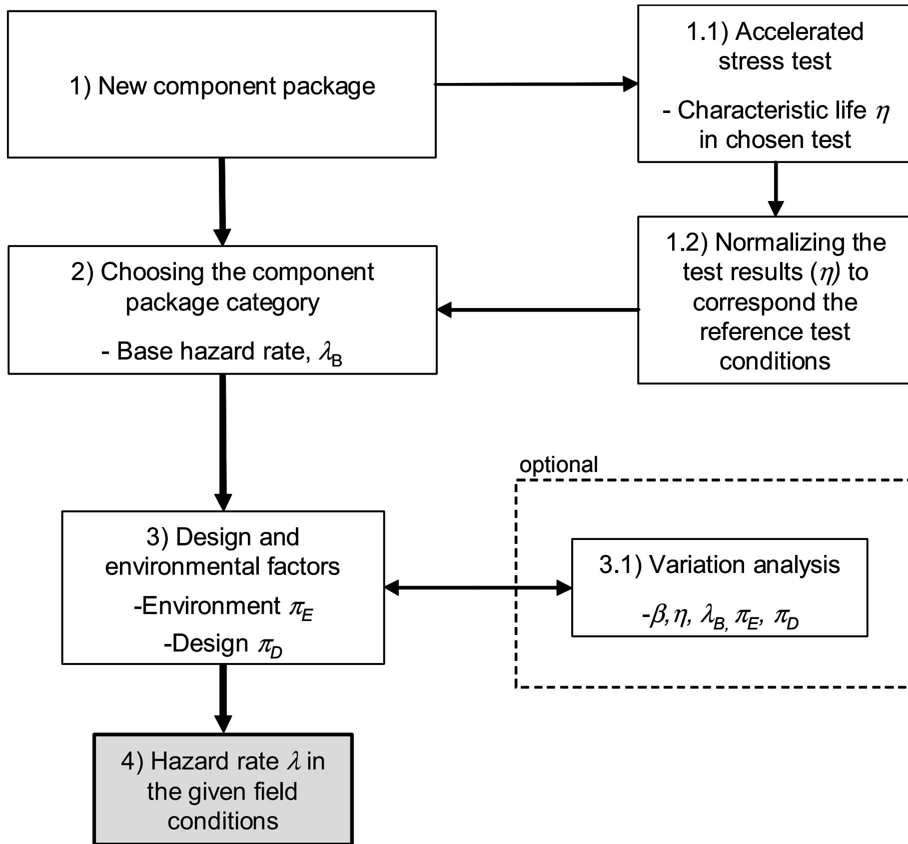

Fig. 12. Process steps of the component package category based analysis. Accelerated stress data is needed for input (1.1). The result (4) is a hazard rate estimation of the component interconnections in the given field conditions. β denotes the Weibull shape parameter.

3.3 Design and environment stress based reliability analysis

In a certain product design phase, there will be a question:"*what is the stress level of the product in the usage environment?*" This is a relevant question, as stresses affect greatly the product design specifications, and from there to every part of the product. The stresses experienced by the products are based on the product design and its usage environment. When millions of products are manufactured and shipped to different geographic locations, one can not say that the stresses

induced to the product by the environment are the same for every product. The effect of the environment can be minimized for example with good thermal management in the product design. However, even with the best designs the stress levels experienced by the individual products will vary. This leads to the situation where the standardized usage environments are irrelevant or at least misleading. After all, there is no clear answer to the aforementioned question. Moreover, this contradiction makes the reliability predictions difficult, as there are at least two unknown parameters in the equation, the reliability and the stress level.

There are ways to overcome this contradiction. First of all, the products could be designed so that they will be operating as intended to with every imaginable usage conditions, with a use of common sense. In the commercial electronics, this is not applicable at all, as the consumers are not willing to pay the increased costs of the higher reliability. However, this approach is used more often in the infrastructure electronics industry. The second option is to make an analysis of the different kind of usage environments and to estimate the risk levels related to the different stress levels. In other words, the stress levels are increased gradually and the failure predictions are made for the particular environment. The stresses are increased at least to the level where the reliability goals are not met anymore. If this stress level is in the range where the products will most probable be used, the product needs modifications. One way to visualize the relation of the stress levels and the expected performance of the product population is to make a response surface chart. The response surface charts can be used for both Backward and Forward Reliability concepts, although the analysis based on the past data is more accurate.

Fig. 13 shows a surface chart of life time expectancy (characteristic life) of the ceramic leadless component as a function of average temperature and the range of daily temperature fluctuation. The component package is a ceramic leadless package (CLLCC). The details of the component can be found in Appendix 1 (Table 49). The characteristic life is calculated with the Engelmaier (1993) method, which is described in detail in the next Chapter. Fig. 13 arrow points to 10 years lifetime expectancy of 63.2% population in the average temperature of 45 °C and with the daily temperature fluctuation of 42 °C. The 63.2% is a failure level at so called characteristic life, and is explained in section 4.1, Equation 19. The results show that if the temperature fluctuations could be decreased by 10 °C the characteristic life would be 17 - 18 years. It can be noted that the lifetime expectancy is more sensitive for the range of daily fluctuation than the average temperature.

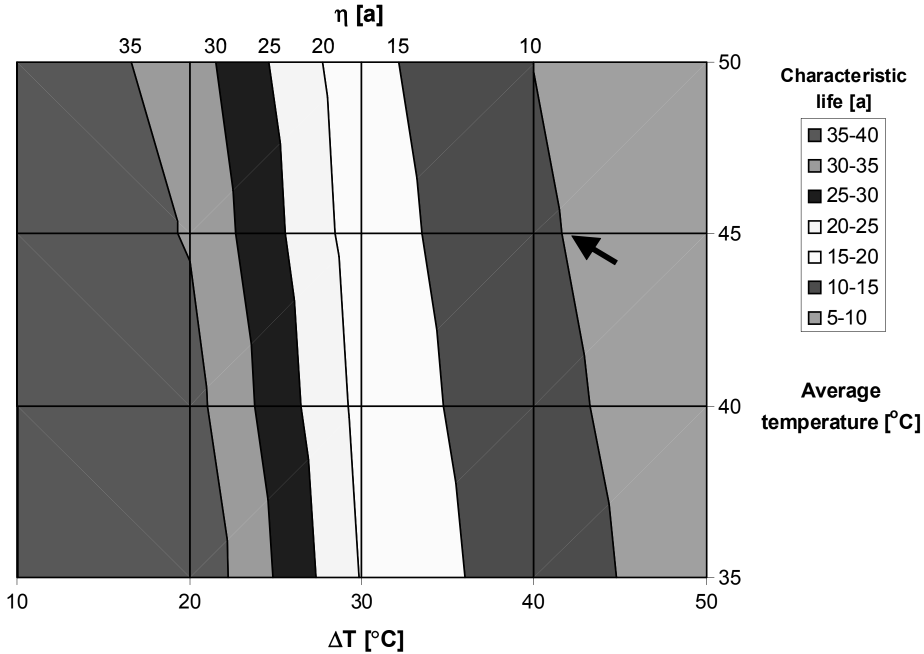

Fig. 13. A surface chart of solder joint lifetime expectancy of a ceramic leadless component (CLLCC) as a function of *ΔT* and average *T*. Arrow points a 10 years lifetime expectancy in the 42 °C temperature fluctuation with 45 °C average temperature. *η* denotes the Weibull characteristic life.

Fig. 14 shows similarly the life time expectancy of the solder joint failures of ceramic leadless component CLLCC, but the cycles per day as the ordinate. The average temperature is fixed to 45 °C. Fig. 14 arrow points to two thermal cycles of 29 °C per day that will result in 10 years of service life, with average temperature of 45 °C. If the lifetime expectancy for the product is *e.g.* 10 years (characteristic life), the stresses experienced by the product should not overlap the zero to ten years area in the Figures 13 and 14. Thus even the worst performing component will maintain its function for a long period of time, when the environment is favourable to it. As a conclusion, the thermal cycling results can not be transformed to the reliability predictions as such. One must know the stresses induced by the environment to be able to predict the reliability of the particular technology.

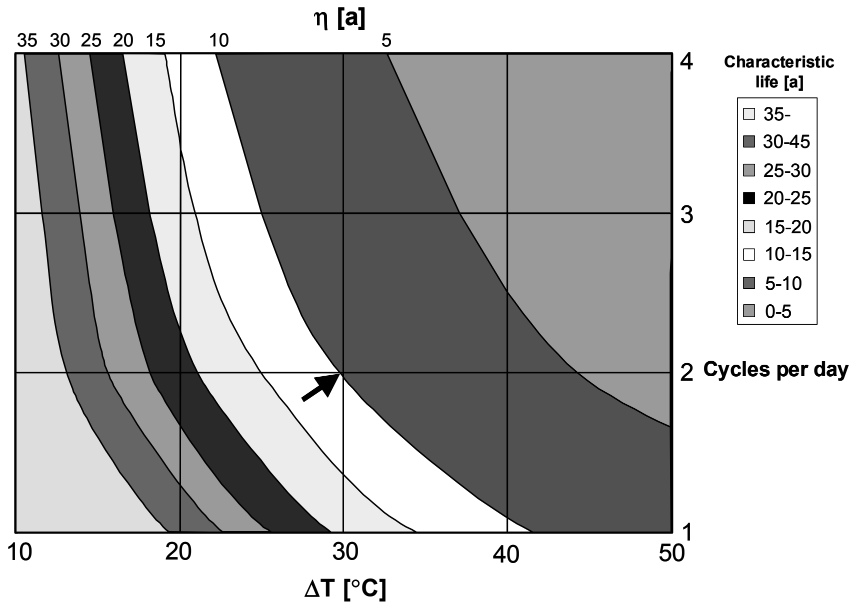

Fig. 14. A surface chart of ceramic leadless components solder joint lifetime expectancy as a function of *ΔT* and number of temperature cycles per day. Arrow points to a 10 years lifetime expectancy in the 29 °C temperature fluctuation with 2 cycles per day. The average temperature is fixed to 45 °C.

3.4 Conclusions

The solder joint management during the product development is a complex task. There are very well known and characterized factors available for the interconnection reliability analysis, but they are seldom utilized. Such factors include for example the material properties of the components and their failing characteristics in the accelerated stress tests. However, there are a variety of parameters that are not accurately known due to their nature. The stress level at the usage environment is one of those. Without knowing the stress levels experienced by the component interconnections, the reliability can not be given exactly. This makes the analysis complex.

The Backward and Forward Reliability concepts were presented. The Backward Reliability methods are based on the knowledge of the field performance of the well known technology, whereas the Forward Reliability lacks

of such information. Even though the stress levels are not accurately known in the individual product level, the experiences from the past products can be utilized. This can be done, when there is only a minor change involved and the stress levels are expected to remain in the same level with the new product generation.

If the stress levels in the usage conditions are not well known, the design and environment stress based analysis method would help to meet the reliability goals. In the stress analysis the stress levels are increased gradually and the failure predictions are made for the particular environment. The stresses are increased at least to the level where the reliability goals are not met anymore. If this stress level is in the range where the products will most probable be used, the product needs modifications. This method could also be denoted as *interconnection stress management*.

The effect of different stress levels on the expected lifetime of component interconnection can be visualized with response surface graphs. They are relatively easy to make and the visual outlook gives enough information for the decision making. Also, the response surface charts give inputs to the thermal management of the product so that the product lifetime requirements are met. They help with the creation of a reliability analysis when the stresses experienced by the products are not well known.

The component package category based assessments utilizes the component package qualification data for the interconnection failure estimates in the given field conditions. The method is described in detail in Chapter 5.

4 Lifetime costs of second level interconnection failures

In this Chapter the solder joint failures are presented in the terms of costs. Solder joint costs can be allocated to design, manufacturing and maintenance costs. In the design phase the emphasis on the costs of the interconnections are still very minor, even though most of the costs in the long term are made in the design phase. The interconnection costs in the design phase are most related on the chosen component technology. The manufacturing costs can generally be addressed to the soldering material costs and the related labour costs. Only a very small fraction of yield loss is purely due to solder joints themselves. The greatest costs related to interconnections can be allocated on the solder joint failures from the field. A failure in a solder joint could lead eventually to failure of an electronics unit, or even the whole system. At this stage the price of one interconnection failure is very high.

In the reliability analysis, the interconnection failures have not usually been transferred to costs. The following sections introduce a novel method to interpret the interconnection reliability performance to long term product costs.

4.1 A study of predicting the second level interconnection failure occurrence

Usually an interconnection reliability analysis consists of thermal cycling data with cumulative failures versus testing time. This is the way the solder joint performance is presented in research publications. The information presented is very useful for the characterization and comparison of a new material or technology. In spite of that the information for the product risk analysis with the real product design and usage environment is very minor. This section concentrates on the solder joint reliability analysis in the different usage conditions. The failure mechanism is expected to be second level solder joint fatigue; other solder joint or component intrinsic failure mechanisms are not a part of this study.

In order to estimate the effect of alternative component packages to the interconnection reliability some basic information from the test laboratories and material sets are needed. These include the material dimension and mechanical properties of the component, the solder and the PWB together with the Weibull characteristic life η from the accelerated stress test. The Weibull shape parameter

β of the laboratory test is not needed as it describes only the quality and reproducibility of the test board and the test itself. Instead, constant Weibull shape figures for leaded and leadless packages are used in this study as suggested by Engelmaier (1993). However, there are many publications where the test shape figures have successfully been used within the interconnection reliability predictions (Särkkä *et al*. 2003, 2004a & 2004b, Salmela *et al.*2003 & 2005).

Also, accurate information of the usage environment is needed, but usually it is based on the standardized product categories. The following study is theoretical, and the material properties and the thermal cycling test performances are not made from experimental data. However, the properties and reliability performance of each of the components is based on the experience of years of testing by the author. All the components are treated in a similar manner described later on. The idea of the study is to walk through the phases which are needed for the complete interconnection reliability analysis.

The study concentrates on a digital electronic device, that consists of four different kinds of components and its estimated lifetime is 10 years with maximum 1% failure level. The component functions needed for the product are processor, memory, oscillator and resistors. The amount of the components depends on the chosen component package type, Table 9. The design does not have any redundancy, meaning that failure with any of the components interconnections will lead to product failure and need for replace the product to a new one. No other costs, *e.g.* transportation or reworking, are expected from the failures. The following interconnection reliability analysis is purely theoretical, due any quality deviations or other customer, product or component dependences are not taken into account. The analysis concentrates on the interconnection reliability of the different component packages.

The parameters of the component packages under study are presented in detail in the Appendix 1 (Table 48 and Table 49). The processor component packages have a minor difference between them; the largest difference is their package size. BGA1 refers to a 27×27 mm^2 Ball Grid Array (BGA) package, which has solder joints in 26 rows, whereas BGA2 refers to a 19×19 mm^2 (18 rows) and BGA3 to a 21×21 mm^2 (20 rows) packages, respectively. The oscillator package options are ceramic leadless chip carries (CLLCC) and leadless plastic package (LLP). The CLLCC_D denotes the dual-in-line type of interconnections, where there are leadless solder castellation in the two sides of the component. The CLLCC_Q refers to a quad type of CLLCC where the joints are on the four sides of the component. The LLP has also the solder castellation in

the four sides of the plastic substrate. These packaging technologies are typical for the oscillator components.

The memory components are divided in to leaded and leadless options. The lead-containing Thin Small Outline Packages (TSOPs) are very popular in the digital electronics. The TSOP_A42 denotes a TSOP package with Ni42Fe alloy (alloy-42) leads. The alloy 42 has a great advantage as lead material, when it is closely attached to silicon or ceramic, as their thermal expansions are close to each other. On the other hand the difference in Coefficient of Thermal Expansion (CTE) of the alloy-42 and the PWB material is large. Moreover, the adhesion between the alloy-42 and solder has been reported to be poor (Fay, Canumalla & Viswanadham 1997). The third option for the memory is a μBGA package, which is smaller in size than the processor BGA packages. These memory packaging technologies are common. The resistors are thin film on alumina ceramic substrate type of chip components with size options of 0201, 0402 and 0603, very common in electronics.

Table 9. The component options for the product. The amount of each components needed to the product is presented in the parenthesis.

	Processor	Memory	Oscillator	Resistor
Package option 1	BGA1	TSOP_A42	CLLCC_D	0201
	(2 x)	(3 x)	(2 x)	(100 x)
Package option 2	BGA2	TSOP_Cu	CLLCC_Q	0402
	(2 x)	(2 x)	(2 x)	(100 x)
Package option 3	BGA3	μBGA	LLP	0603
	(1 x)	(1 x)	(1 x)	(100 x)

To predict the product failures caused by the component interconnections, the effects of design and usage environment on the interconnection reliability must be estimated. Table 10 shows different usage environments experienced by the product, namely *the desktop PC, the installed telecom* and *the portable telecom* (HDPUG 1999). The *portable telecom* –field category has the lowest difference in temperature, but has multiple cycles per day, whereas the other two field categories have a slightly higher temperature range. The temperature fluctuation causes thermo mechanical stresses to the solder joints, which causes the aging of the joints. No other stress conditions, *i.e.* vibration, are taken into account. Without any deeper analysis, it would be impossible to tell whether the amount or the range of the temperature fluctuations gives more stress to the solder joints.

Furthermore, it cannot be said whether the components will maintain their performance during the required service life or not.

Table 10. Design and usage environments by HDPUG (1999).

Environment category	Environment device category	Daily Temperature Fluctuation, ΔT	Cycles Per Day (CPD)
Indoor, temperature controlled	Desktop PC	35 °C	2
Outdoor, Unprotected	Portable Telecom	30 °C	24
Outdoor, Protected	Installed Telecom	45 °C	1

In order to predict the component interconnection failures during their lifetime in different usage conditions, the component thermal cycling test hazard rates are interpreted to correspond to the hazard rates in the different field conditions. This can be done by estimating the acceleration factor between the stresses in the test and in the field. The commonly used method for estimating the stresses induced by cyclic loading is introduced by Engelmaier (1993), who divided the prediction models into two different parts. The model to be used is chosen whether the stress levels seen by the solder is below or above the yield strength of the solder. The solder joints of leadless components typically reach higher stresses and they are generally considered to exceed the yield strength. The leaded components are then under another model, as their solder joint experience relatively lower stresses. (Engelmaier 1993). Both models, with recent updates referred to the lead-free solder, are used in the study.

The fatigue life $N_f(x\text{-}\%)$ at a given failure probability x of surface mount solder attachment is written (Engelmaier 1993) by

$$N_f(x-\%) = \frac{1}{2}\left(\frac{\Delta D}{2\varepsilon_f^{'}}\right)^{1/c}\left(\frac{\ln(1-0.01x)}{\ln 0.5}\right)^{1/\beta}, \tag{10}$$

where ΔD is a cyclic fatigue damage, $\varepsilon_f^{'}$ is a fatigue ductility coefficient and β is the Weibull shape parameter. The fatigue ductility exponent c is written

$$c = -0.442 - 6\times10^{-4}T_{SJ} + 1.74\times10^{-2}\ln\left(1+\frac{360}{t_D}\right), \tag{11}$$

in where T_{SJ} is a mean cyclic solder joint temperature and t_D is a half cycle dwell time. As stated, the term ΔD is the measure of the cyclic fatigue damage. For leadless and leaded solder attachments it is written

$$\Delta D_{leadless} = \left[\frac{F_u L_D \Delta\alpha \Delta T_e}{h} \right] \quad (12)$$

and

$$\Delta D_{leaded} = \left[\frac{F_u K_D \left(L_D \Delta\alpha \Delta T_e \right)^2}{1.38 MPa \times Ah} \right], \quad (13)$$

respectively, in where the equivalent cycling temperature swing ΔT_e is

$$\Delta T_e = \left| \frac{\alpha_s \Delta T_s - \alpha_c \Delta T_c}{\Delta\alpha} \right| \quad (14)$$

and

F_u	unideality factor,
$2L_D$	maximum distance between the solder joints of component,
$\Delta\alpha$	difference in CTE of component and substrate,
ΔT_s, ΔT_c	cyclic temperature swing of substrate and component,
α_s, α_c	CTE of substrate and component,
h	effective solder joint height,
K_D	diagonal flexural strength and
A	effective solder joint area, definitely 2/3 of solder wetted area.

It is assumed that temperature changes are relatively slow and the temperature is evenly distributed in the component and the substrate so that ΔT_S equals ΔT_C . This will result the Equation 14 to

$$\Delta T_e = \Delta T_S = \Delta T_C. \quad (15)$$

For the lead free solder SnAgCu, the unideality factor is set to 1 and the fatigue ductility coefficient is replaced with the stress dependent correction term *corr* (ΔT) is

$$corr\left(\Delta T\right) = A_s \cdot \ln\left(\Delta T\right) + B_s, \quad (16)$$

where ΔT is the temperature difference and A_s and B_s are component and material specific constants as shown in Table 11 (Salmela *et al.* 2006). The correction term is needed to add a temperature dependency to the fatigue ductility coefficient to better describe the behaviour of SnAgCu solder in different stress levels. The correction term is used only for the leadless components in this study.

Table 11. Material constants A_s and B_s of the stress dependent fatigue ductility coefficient for non-leaded components (Salmela *et al.* 2006).

Package & solder materials	Type of joint	A_s	B_s
Ceramic, SnAgCu	Leadless	0.0884	0.130
Plastic, SnAgCu	Leadless	0.179	–0.0953
Plastic, SnAgCu	BGA	0.149	–0.0794

The component parameters are presented in detail in Appendix 1 (Table 48 and Table 49). The estimated performance in test conditions of each component is presented in Table 12.

Table 12. Estimated characteristic life η in thermal cycling test for each component package under study. As reference, the IPC-9701 standard prefers 1000 cycles for solder attachments in –40 °C to +125 °C thermal cycling test.

	Processor			Memory		
	BGA1	BGA2	BGA3	TSOP_A42	TSOP_Cu	BGA
η [thermal cycles]	2819	1629	4243	848	4570	825

	Oscillator			Resistor		
	CLLCC_D	CLLCC_Q	LLP	0201	0402	0603
η [thermal cycles]	657	266	5338	4511	3492	1917

It can be seen that one of the component packages in each component category is superior when compared to others. Usually the usage decision is based on functionality and cost, and the interconnection reliability concerns are omitted. The component package for processors should be easily chosen, as all the processor-BGAs are fulfilling the requirements specified in IPC-9701 (2002), so that their characteristic life is at least 1000 thermal cycles. Also, the choosing of the memory component should be simple as the interconnections of the TSOP_Cu have five time higher lifetime expectancy than the other two. The oscillator case seems to clear from interconnection reliability point of view, but the designer might save in component cost if he/she chooses the leadless ceramic packages instead of the high reliable plastic package. Usually there is a pressure from the electrical performance point of view, which in this case is the stability of the substrate and superior electrical performance of the ceramic package. The resistors are chosen usually for the electrical performance and the needed space

point of views with the cost reduction in mind. In spite of that, the thermal cycling performance should make this choice easier.

Table 13. Characteristic lifetime (63.2% failure level) of each component in the different usage environments. The components with less than 10 years characteristic life expectation should be rejected from usage and 10 to 32 years should be considered as high risk components.

Field category	Processor			Memory		
	BGA1	BGA2	BGA3	TSOP_A42	TSOP_Cu	μBGA
Installed telecom	27.3	16.7	39.4	327.1	1491	9.0
Portable telecom	6.3	3.6	9.4	362.6	1943	1.8
Desktop PC	23.3	14.1	33.9	606.9	2833	7.6

Field category	Oscillator			Resistor		
	CLLCC_D	CLLCC_Q	LLP	0201	0402	0603
Installed telecom	9.4	4.2	48.5	53.5	42.5	24.7
Portable telecom	2.2	0.9	11.8	15.0	11.6	6.4
Desktop PC	8.5	3.7	41.8	49.4	39.1	22.6

The Equation 10 was utilized to estimate the characteristic life of the aforementioned components in the field conditions specified in the Table 10. The characteristic lifetimes of each component interconnections are listed in Table 13. The numbers denote when statistically 63.2% of the components have failed due to the solder joints. To achieve a maximum 1% failure level during the designed lifetime of 10 years, the characteristic life should be 32 years with $\beta = 4$ (per Equation 10). The time to 1% solder joint failure of each component is listed in Table 14. So, the components whose predicted characteristic life is 10 years or less should be rejected without hesitation. Also, the components within 10 to 32 years life time should be concerned as high risk components, as up to 63.2% is predicted to fail during the product lifetime of 10 years. Keeping that as a design rule, the *portable telecom*-field category (HDPUG 1999) seems to be too severe for most of the components under study.

Table 14. Time to 1% interconnection failure level of each component in the three given usage conditions. 10 years lifetime with maximum of 1% failure level was specified for the product with shape parameter of 2 and 4 were used for leaded and leadless attachments, respectively.

Field category	Processor			Memory		
	BGA1	BGA2	BGA3	TSOP_A42	TSOP_Cu	μBGA
Installed telecom	8.7	5.3	12.6	3.3	15	2.9
Portable telecom	2.0	1.2	3.0	3.6	19	0.6
Desktop PC	7.5	4.5	10.8	6.1	28	2.4

Field category	Oscillator			Resistor		
	CLLCC_D	CLLCC_Q	LLP	0201	0402	0603
Installed telecom	3.0	1.3	15.5	17.1	13.6	7.9
Portable telecom	0.7	0.3	3.8	4.8	3.7	2.0
Desktop PC	2.7	1.2	13.4	15.8	12.5	7.2

Furthermore, most of the processor components can be categorized as high risk components due to their interconnections. The memory package μBGA seems not to be a good option for the product as the TSOPs are superior. Although, the characteristic life expectation for the TSOPs are so high that their interconnections should not be any concern at all. This is resulted from the Equation 13, where the strain parameter is squared and the acceleration factor will be a lot higher than with leadless components. However, the life expectations for alloy-42 leaded TSOPs are far too high. The local CTE mismatch with alloy-42 lead and the PWB would accelerate the failing of the TSOPs (Clech *et al.* 1993). This is not taken into consideration in Equation 10, and shorter lifetime should be expected. In the oscillator area, the leadless plastic package seems to be the superior option. The resistors seem not to be the most risky components, although the 0603 resistor might not be chosen for the products intended for the portable telecom field category for 10 years.

To estimate the reliability of each component to maintain its proper function for 10 years service life, the failures were expected to follow the Weibull distribution. The corresponding reliability function *R(t)* is

$$R(t) = e^{-\left(\frac{t}{\eta}\right)^{\beta}}, \tag{17}$$

where t, η and β are the corresponding time, characteristic time and Weibull shape parameter, respectively. The Weibull distribution is used widely when fitting the test results, as it can be adjusted to fit many life distributions (Weibull 1939). It is suggested to use values $\beta = 4$ and $\beta = 2$ for leadless and leaded SnPb attachments, respectively (Engelmaier 1993). In this analysis the aforementioned values are used for the Weibull shape parameters of the SnAgCu-solder, although $\beta = 3$ value has also been suggested for SnAgCu solder (Salmela *et al.* 2005, Engelmaier 2007).

The interconnection reliability, $R_{int_component}$, of each component during the 10 years life time is shown in Table 15. The analysis shows that the component packages for the processor, the memory, the oscillator and the resistors can be chosen so that ≥ 99% reliability levels (≤ 1% failure level) are met for 10 years of operation. The random and overstress failures are naturally excluded from the analysis. The results also show that the *portable telecom*-environment category is far too severe for the solder joints of most of the component packages, Table 15. Furthermore, the µBGA-memory and the ceramic oscillators (CLLCCs) should not be used in any of the three field categories for 10 years lifetime.

The product level reliability estimation can be derived from the component level reliability estimations. Equation 3 was used for the total interconnection reliability estimates. The probability that the product consisting of components from Table 9, will maintain its function for 5 and 10 years in given field conditions is presented in Table 16. The table shows the total interconnection reliability when the component package is chosen with minimum, average and maximum performance in each component category. The reliability analysis shows that the component packages do have a great difference when interconnection reliability is taken into account. The 99% reliability can be met in the *installed telecom* and *Desktop PC* field categories for 5 years, but 88% is the maximum achievable interconnection reliability for 10 years service life. Furthermore, only the best performing components are adequate for the product, whereas the others have far too high failure expectations.

Table 15. Interconnection reliability (%) $R_{int_component}$ of each component type for 10 years life time.

Field category	Processor			Memory		
	BGA1	BGA2	BGA3	TSOP_A42	TSOP_Cu	μBGA
Installed telecom	98.21	87.80	99.59	100.00	100.00	22.09
Portable telecom	0.15	0.00	27.82	100.00	100.00	0.00
Desktop PC	96.66	77.67	99.24	100.00	100.00	4.74

Field category	Oscillator			Resistor		
	CLLCC_D	CLLCC_Q	LLP	0201	0402	0603
Installed telecom	28.41	0.00	99.82	99.88	99.69	97.37
Portable telecom	0.00	0.00	59.90	81.87	57.41	0.23
Desktop PC	14.64	0.00	99.67	99.83	99.57	96.24

Table 16. Total interconnection reliability (%) of 5 and 10 years of service.

Field category	5 years			10 years		
	Min.	Avg.	Max.	Min.	Avg.	Max.
Installed telecom	1.3	57	99	0.0	14	88
Portable telecom	0.0	1.0	26	0.0	0.0	0.0
Desktop PC	0.1	51	99	0.0	9.9	84

The product level interconnection reliability analysis can also be divided into smaller parts to estimate the effect of the different components in the system. In order to get a larger view of the differences in the interconnection reliability performance of each component package, a graph of cumulative failures of each component was plotted. The failure expectation *F(t)* at a given time *t*, which is also denoted as unreliability, is derived from a formula

$$R(t) + F(t) = 1, \tag{18}$$

where *R(t)* is reliability at a given time. The *F(t)* is also denoted as cumulative distribution function (c.d.f), and is written

$$F(t) = 1 - R(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}}, \tag{19}$$

where η and β are the Weibull characteristic life and shape parameter, respectively. Equation 19 was used for the cumulative failure plotting of each component. At the particular time, when $t = \eta$, the Equation 19 will get a value of

F(t) = 0.632, independently from shape parameter *β*. So, the Weibull characteristic life can be read from cumulative failure plots, where the failure level reaches 63.2%. The interconnection cdf curvatures show the difference of the component package options in graphical form and can very easily be communicated to the product designers. The curvatures help designers to get maximum performance out of the product without catastrophic failures during the designed lifetime. It also helps finding the optimum in performance and reliability. This is the core of this analysis. Such analysis can not be found from the usual reliability analysis, where only the thermal cycling test data is presented and no interpretation to field conditions are done.

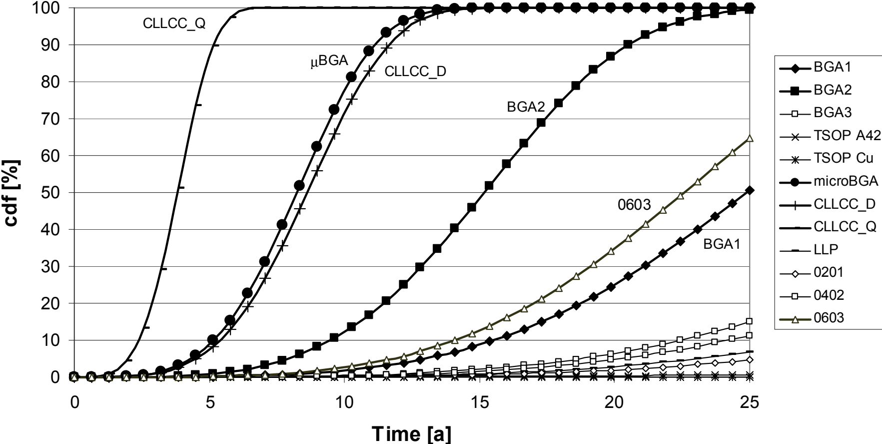

Fig. 15. The cumulative failures (cdf) of the component interconnections as a function of time in the *installed telecom* field conditions. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

Fig. 15 shows cumulative failures of each component in the *installed telecom* field category and Fig. 16 in the *desktop PC* field category. The figures show that the μBGA and both ceramic leadless oscillators are failing far before the specified ten years service life. It can also be noted, that the cumulative distribution functions of each component in the *installed telecom* and *desktop PC* are quite similar. Furthermore, it can be noted that the quad type ceramic oscillator (CLLCC_Q) does not fulfil even five years life expectation. Within the oscillator category, the plastic substrate oscillator (LLP) is superior in terms of interconnection reliability. As a conclusion, the interconnection reliability of most

of the components would be at least adequate in the *Installed Telecom-* and *Desktop PC* field categories. The analysis shows that the ceramic oscillators (CLLCC_Q and CLLCC_D), the μBGA memory and the BGA2 processor should not be chosen for the product under the study.

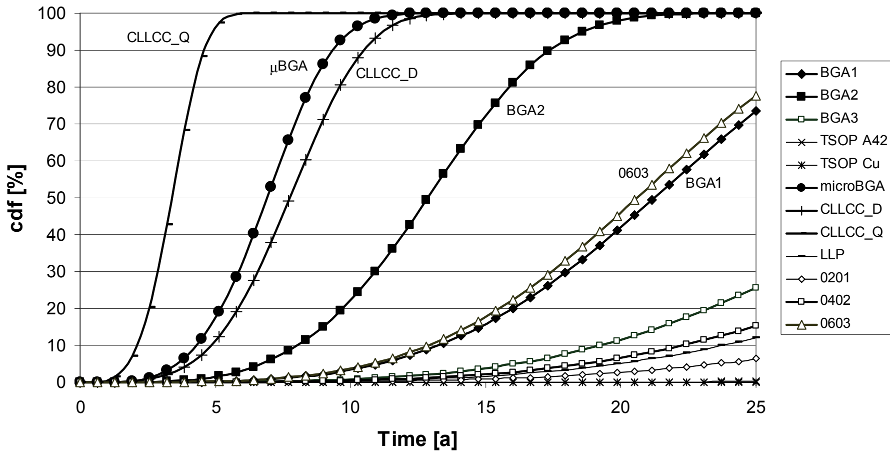

Fig. 16. The cumulative failures (cdf) of the component interconnections as a function of time in the *Desktop PC* field conditions. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

The zero reliability expectation in the product level in the *portable telecom* field category is explained by the bad interconnection reliability performance of 10 out of 12 components. The only components without significant failures are the leaded TSOP-memories, whose relatively good performance was explained earlier. Thus 10 years in the specified *portable telecom environment* is very demanding for most of the components under investigation, as can be seen from Fig. 17. To compare the stresses of the three field conditions, the BGA3 processor has 0.5–0.8% failure expectation in the *installed telecom* and *desktop PC* field categories, whereas the failure level of 75% in the *portable telecom* field category is expected at the 10 years of service. Furthermore, the failure level of 1% is expected after only three years in the *portable telecom* field category.

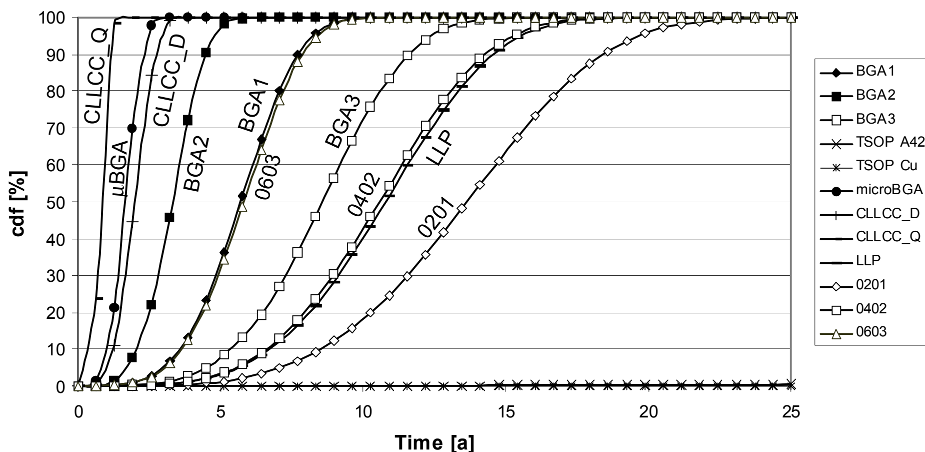

Fig. 17. The cumulative failures (cdf) of the component interconnections as a function of time in the *portable telecom* field conditions. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

To further investigate the interconnection failures in the product level during the time in the field, the interconnection failures are presented as hazard rates at given time. As the Weibull distribution was expected to describe the interconnection failure occurrence, they can be further processed with the Weibull methods. The hazard rate *h(t)* of the two-parameter Weibull distribution is

$$h(t) = \left(\frac{\beta}{\eta^{\beta}}\right) t^{\beta-1}, \tag{20}$$

where β, η and t are the shape parameter, characteristic life parameter and time, respectively. The unit for *hazard rate* is the amount of failure occurrences in time. The *hazard rate* of Weibull distribution should be distinguished from the *constant hazard rate*, λ, of the exponential distribution, (O'Connor 1999). For repairable systems, λ is also referred to as *failure rate* and $1/\lambda$ is called Mean Time Between Failures (MTBF). The unit for λ is Failures-In-Time (FIT), meaning the amount of failures per 10^9 service hours. The MTBF is used for repairable systems, where as Mean Time To Failure (MTTF) is used for non-repairable systems (O'Connor 1999). The FIT figure usage for the interconnection elements has been a minor activity. In spite of that the solder joint hazard rates have been presented in MIL-HDBK-217F (1991).

Fig. 18 shows the hazard rate of BGA1 in the three given field conditions in ten years. For reference, the typical component intrinsic FIT figure levels for processors are under 100 (Freescale 1999). The hazard rates of Weibull and exponential distributions are not comparable to each other as such due to their different distribution models. However the comparison could give a certain reference level for the interconnection hazard rates. This value (100 FITs) is clearly exceeded only in the *portable telecom* environment. The interconnection failures exceed 100 FITs after 4 years of service. After that, the interconnection failures should occur more often than the component intrinsic failures. So, the interconnection failure modes become the dominant failure mode above that. After 5 years in the *installed telecom* environment, the BGA1 has reached a hazard rate of 1 FIT, meaning that there will be one failure per 10^9 hours of service in the product population or one fail per 1×10^9 cumulative hours.

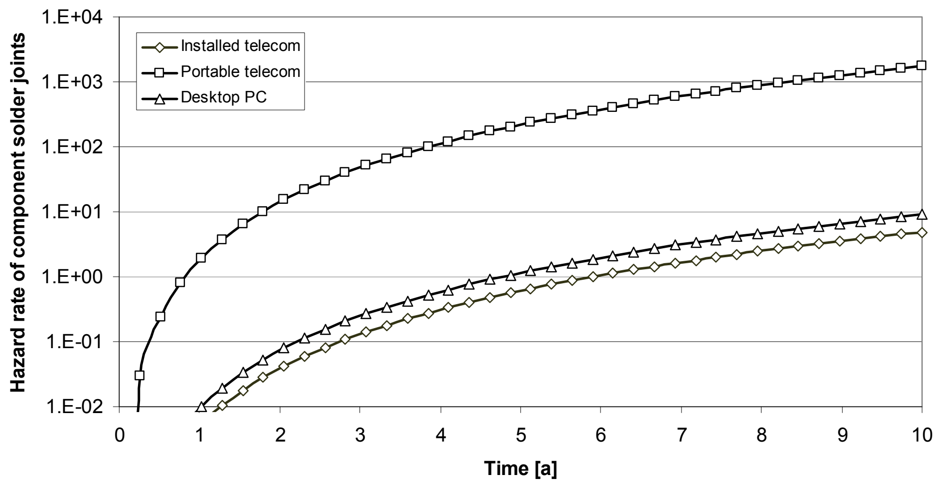

Fig. 18. Interconnection hazard rate (FITs) of BGA1 component in the three field environments per Weibull distribution. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

To conclude, the component interconnection reliability analysis is a powerful tool when estimating the interconnection failures of the product. The estimated lifetimes can be compared in the different usage environments in graphical form and are very easy to communicate to product designers instead of showing the standard cumulative failures versus time in a test chamber graph. In the analysis

method, the component packaging qualification data is interpreted into clear failure expectations in the given usage environments.

Aforementioned analysis is much more comprehensive and sophisticated than the commonly published interconnection reliability analysis, where only the thermal cycling data is presented without any interpretation to common field environments.

4.2 Costs of interconnection failures

In this Section, a novel analysis method of interconnection failure costs is presented. Such analysis, where interconnection elements are dealt as cost elements, has not been reported earlier according to the author's best knowledge. The purpose of this analysis is to bring the engineering reliability methods closer to the economics analysis, although the latter one is presented here in a very simplified manner. The idea is to allocate a cost for an interconnection failure, which enables comparison between the different component packages with respect to life time costs.

As stated in the previous Section, the component failure will lead to product change with Standard Product Cost (SPC) of the product. In this analysis only the material costs of components are included in the SPC. The purchasing prices of each component are shown in Table 17.

Table 17. The component cost alternatives used in the analysis. The component costs are exemplary, but follow component prices related to given component types.

Processor			Memory		
BGA1	BGA2	BGA3	TSOP_A42	TSOP_Cu	µBGA
2 × 11 € = 22 €	2 × 12 € = 24 €	1 × 21 €	3 × 4 € = 12 €	2 × 5 € = 10 €	1 × 9 €

Oscillator			Resistor		
CLLCC_D	CLLCC_Q	LLP	0201	0402	0603
2 × 2 € = 4 €	2 × 2 € = 4 €	1 × 5 €	100 × 0.01 € = 1 €	100 × 0.01 € = 1 €	100 × 0.009 € = 0.9 €

The component costs shown in Table 17 are exemplary, but they follow component prices related to given component types. The actual price of the product components is based on negotiations, as well as on the economics of scale. Due to this their exact value can not be given in the longer time frame. An online electronics catalogue can be found via reference Jameco Electronics (2008). The amount of each component was specified in Table 9. Depending on the chosen components, the total component cost of the product would be from 34.9 € to 42 €. The lowest material cost would be achieved with one BGA3 processor, one µBGA memory, either of the two CLLCC oscillators and 100 of 0603 resistors, Table 17. Moreover, there are 81 possible component variations altogether. The product component costs as a function of interconnection reliability of these 81 variations for ten years in the *installed telecom* field conditions is presented in Fig. 19. The results show that the 27 different component variations results to zero reliability for ten years life time. The components can be chosen four times so that the required ≥ 99% is achieved. The product component costs of these four component sets are from 37 € to 39 €.

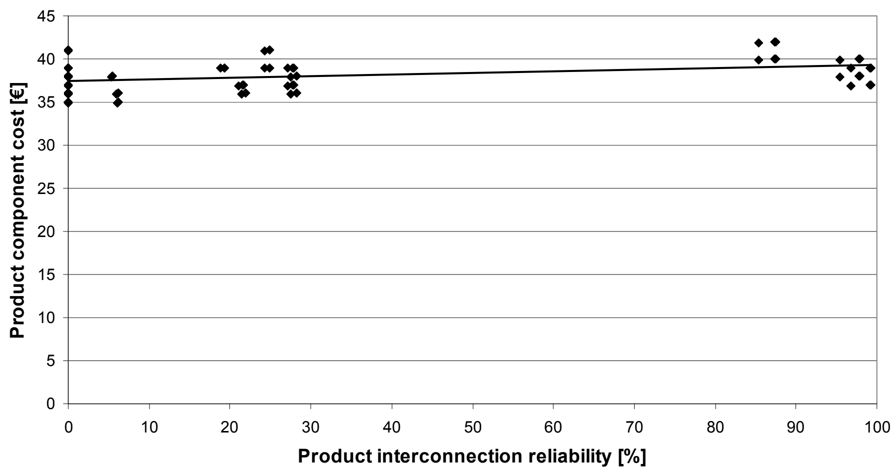

Fig. 19. Component cost of the product as a function of the product interconnection reliability in the *installed telecom* field conditions in 10 years. The product consists of four different types of components, which all have three packaging alternatives. All the possible component variations in the product are plotted (81 variations). 27 component variations result with 0% reliability and only 4 variation results to required over 99% reliability.

The component interconnection failures are transferred to costs by first calculating the interconnection reliability of each component in 10 years service life. The results are shown in Table 15. The total interconnection reliability of each component type $R_{component_type}$ in the non-redundant system is calculated by

$$R_{component_type}(t) = \prod_{i=1}^{n_c} R_{i,component}(t), \tag{21}$$

where n_c is the amount of components in one product, listed in Table 9. The probability that failure will occur in the given period of time is calculated from the reliability figures and is then

$$F(t) = 1 - R(t) = 1 - \prod_{i=1}^{n_c} R_{i,component}(t) \, . \tag{22}$$

The material cost *C(t)* of the failed products is calculated by multiplying the amount of manufactured products n_p with the estimated failures and the material cost of one product by

$$C(t) = n_p \times c_{spc} \times F(t) = n_p \times c_{spc}(t) \times \left(1 - \prod_{i=1}^{n_c} R_{i,component}(t)\right), \tag{23}$$

where $c_{SPC}(t)$ is the standard product cost. The costs related to $c_{SPC}(t)$ will change during the time due to a reduce with migration of the designs along the learning curve. If it is assumed that all the components with same type have exact the same reliability, the Equation 23 can be written:

$$C(t) = n_p \times c_{SPC}(t) \times \left(1 - e^{-\left(\frac{t}{\eta}\right)^{\beta \times n_c}}\right), \tag{24}$$

where η, β and t are the characteristic life, shape parameter and time of the Weibull distribution, respectively. Equation 24 describes the sum of component costs of the failed products, which in this analysis denotes the material costs of the product. It also describes the extra costs within the designed lifetime of ten years, as the failed product is replaced with a new one. No other dependencies in costs structure are taken into account.

The failure costs for 1000 products as a function of interconnection reliability are presented in Fig. 20, where Equation 24 was used. The analysis is made for 1000 products, with a product selling price of 80 €, which is 45 € more than the lowest component cost. This value will later be referred to as *profit*; though it is

an over-optimistic approach. In Fig. 20, only the average product component price has been used for simplicity. In the chart, the Min R, Average R and Max R represent the minimum, average and maximum interconnection reliability performance of the components, denoted in Section 4.1. The results show that with the maximum interconnection reliability the failure costs are around 5000 € after 10 years of service. The life cycle costs for the product are still positive. However, the worst performing components would be exceeding the profit after 5 years of service and even the product income after 9 years.

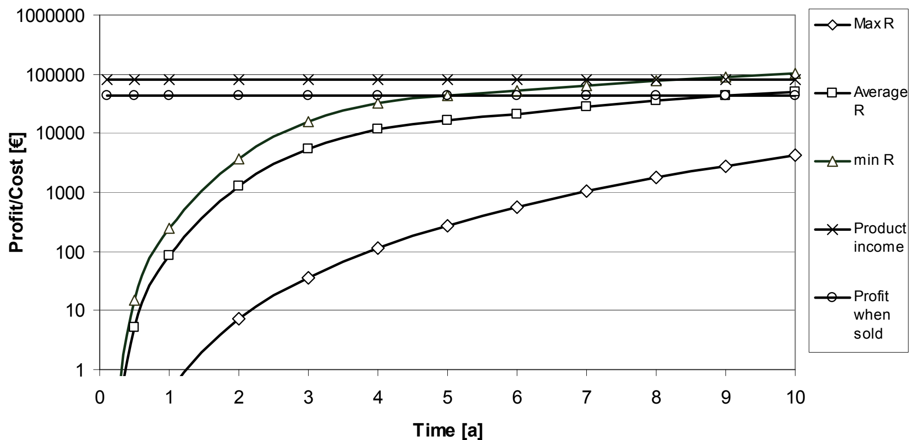

Fig. 20. Additional costs as a function of time in terms of interconnection reliability. The costs are due to the product replacement followed by an interconnection failure. Min R, Average R and Max R denote the interconnection reliability performance of the component types in the four component categories. Only component material costs are taken into account. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

Since the product selling price is the same regardless of the component costs, the *profit when sold* depends on the chosen components. On the other hand the reliability depends on the chosen components and thus the relationship between profit and reliability exists. Fig. 21 shows the profit and costs as a function of total interconnection reliability of the product after 10 years in the *installed telecom* field conditions. The components with minimum, average and maximum interconnection reliability were chosen from each component category for the analysis, Table 15. The results show that the product with the lowest component

material cost (*Product direct costs)* will result in very high negative *profit* (loss) after 10 years.

The ultimate goal for the profit is to at least fulfil the long term operational profit target, which means to exceed the *other costs*. The results show that the *profit at 10 years* will exceed than the *other costs* with approximately 80% interconnection reliability of the product. This reliability level should be considered as a minimum reliability goal. Above 80% interconnection reliability, the long term cash flow is positive; the *acceptable failure costs* region in Fig. 21. As a reference, a comprehensive life-cycle cost analysis made for CD-Radios shows minimum total cost with product reliability of 91% (Kleyner, Sandborn & Boyle 2004). However, there will be no profit at the interconnection reliability level of 17%.

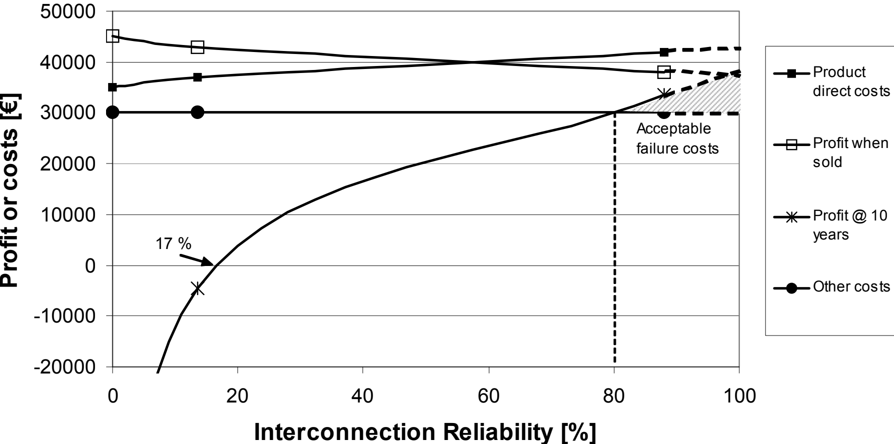

Fig. 21. Profit and costs of 1000 products after 10 years lifetime as a function of interconnection reliability of the four different component sets in *installed telecom-*field conditions. The acceptable failure costs refer to the level of reliability, when the long term profit exceeds the other costs related to the product. The long term cash flow is positive above the 80% interconnection reliability. The profit at 10 years is totally lost with 17% interconnection reliability. Weibull shape parameters of 2 and 4 where used for leaded and leaded connection media, respectively.

The traditional view of reliability and related life cycle costs suggests that reliability and cost can be optimised. On the other hand, the modern view emphasizes that the life cycle costs will be minimized when reliability approaches

to 100%. (O’Connor 1999). The *Profit at 10 years* reaches its maximum at the 100% product interconnection reliability, Fig. 21

Fig. 22 shows the material costs of a product as a function of interconnection reliability. The results show that the highest reliability for 10 years in the *installed telecom* and *desktop PC* –field categories is achieved with component cost of 42 €. The *portable telecom* field category gives zero reliability with all the component sets.

Keeping the earlier mentioned 80% interconnection reliability in the product level as a guideline, the BGA1 and BGA3 processors, both TSOP memories, LLP oscillator and 0201 resistors should be chosen for the product. The decision is based on the long term interconnection reliability and life-cycle costs. The life-cycle costs of the interconnection failures in the *portable telecom* field category are far too high for the components under study.

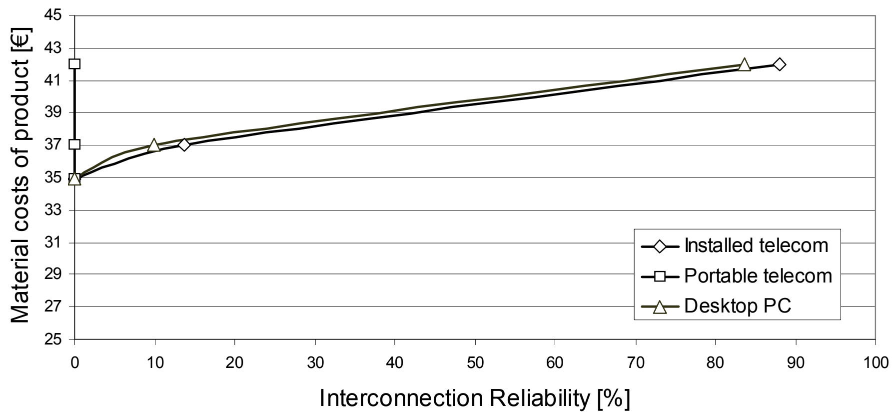

Fig. 22. The component costs of the product as a function of interconnection reliability. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

4.3 Conclusions

A novel method to estimate the interconnection failures in terms of costs was presented. The reliability and cost analysis shows that when comparing the component packages performance with each other and against the requirements, a comprehensive analysis is needed to fully understand the risks involved. The analyses also show that the stress environment must be known accurately, or the costs of the interconnection failures could be tremendous. The cheapest component in the design phase might not necessarily be economically beneficial in the long term due to possible higher failure or maintenance costs.

By knowing the product reliability and the related costs, the selling price of the product can be defined effectively. The life cycle thinking has been a concept in product level management, but the interconnection reliability analyses are not a part of it. One reason for this is that there are no practical tools available during the design processes. Without corresponding analysis, the component interconnection failures might cost more than profit of the product. So, emphasis must be on component selections.

The *installed telecom* and the *desktop PC* field categories look at first to have somewhat minor differences, 10 °C difference in temperature fluctuation and one to two fluctuations cycles per day. In fact, the results of the analysis show that these two environment categories are very similar, when interconnection performance and stress levels are compared to each other. The *portable telecom* field category was chosen as a reference for the aforementioned categories. In this category, the stresses experienced by the component interconnections were very high due to the amount of temperature cycles per day, even though the temperature change is quite minor.

In practise the interconnection reliability cannot be 100%, as there are always quality deviations in components, materials and manufacturing processes. So, additional cost of quality deviations should be added to the analysis. Furthermore, there are other cost elements, which were not a part of this study, but which would have a major part in larger scale cost analysis. Examples of such cost related topics in the interconnection area are a redundancy in design and the rework possibilities of components.

Component interconnection reliability analysis is a powerful tool when estimating the interconnection failures of the product. The estimated lifetimes can be compared in the different usage environments in the graphical form and are

very easy to communicate to product designers instead of showing the standard cumulative failures versus time in test chamber graph.

This analysis method is strongly recommended to be further developed, as it has great potential in product development. More emphasis could be put to find the corresponding cost model for the interconnections.

5 New method for second level interconnection hazard rate estimates

In this Chapter, a novel method to estimate the failure occurrence of component second level interconnections is presented. In the method, the accelerated stress test results of component interconnections are used as a starting point for hazard rate estimates.

The reliability analysis of the component interconnections can be based on the empirical test results or modelling. The empirical test data is preferred as it gives a solid starting point for the analysis with multiple parameters that are difficult to model. These include the geometrical dimensions of the solder lands, the surface finish material, the effect of the other components in the PWB and many others. The disadvantage with the purely model based assessments are the multiple smaller-level parameters that can not be taken into consideration in the models. In the empirical tests these parameters are built-in in the test specimen and are already solidly in the test results. The modelling is very efficient when the effects of particular parameters are estimated and most of the parameter values are known. Smith and Womack (2004) proposed that the empirical models could give accurate predictions of the electronics devices, although the field failures caused by the solder joints were not described in detail.

The earlier published methods for the interconnection failure occurrences rely on the empirical data and are generalized at the component function level (Clech *et al.* 1993, Iannuzzelli 1993 & 1997, Engelmaier 1993, MIL-HDBK-217F 1991, RIAC 2006). These models take into account the operational conditions at a general level, but the accurate information about the component packaging technology itself is neglected. As will be shown the component packaging and its geometrical dimensions have a great effect on interconnection reliability. Recently published parametric model to predict characteristic life of Flip Chip (FC) interconnections in the given conditions was developed by Lall, Singh, Strickland, Blanche & Suhling (2005). In the model, the time to 63.2% failure is dependent on seven different parameters, *e.g.* geometrical dimensions of the solder and temperature range (Lall *et al.* 2005).

As stated in the Introduction, the trend in the characteristic life of the component interconnections in the thermal cycling test has been decreasing remarkably in the last two decades. In spite of that, the public knowledge of solder joint failures has not reached the surface. There can be two explanations for this, either solder joint failures do not figure as one of the most important

failure mechanisms of the electronics products or such information has not been collected. For the latter, a sophisticated method to estimate the solder joint failures is needed, in order to avoid catastrophic component failures during their designed life-time.

The failure occurrence in the particular field conditions are estimated based on the readily calculated values. The resulted accurate failure occurrence figures can be used as a part of the reliability analysis of the whole product. Also, novel methods for assessing the reliability performance in the product level are presented. In these methods, the estimated operational stresses are taken into account instead of just relying in the qualification only on the data from accelerated stress tests. This is more of the "fact-based-management" than the commonly used zero failures within 1000 thermal cycles qualification criterion.

5.1 The interconnection failures-in-time

Solder joint failure is a result of solder fatigue caused *i.e.* by the frequent thermal fluctuations. This is usually due to the thermo-mechanical incompatibility of the interconnection system, which induces stresses to the solder joints during the thermal fluctuations. The stress initiates the solder joint fracture, which propagates to full rupture and to failure of the interconnection. The component level failure occurrences, or hazard rate, increase with time. The hazard rate follows the two-parameter Weibull distribution, which is used in this thesis to describe the behaviour of the interconnection failures in time (iFIT).

Constant hazard rate is commonly expected with the component intrinsic failures (*e.g.* MIL-HDBK-217F 1991), which is based on the exponential distribution model (O'Connor 1999). The hazard rate *h(t)* of the exponential distributions is written

$$h(t) = \lambda, \tag{25}$$

where λ is the number of failures per 109 hours (FITs). The hazard rate of the exponential distribution gives the same level of failures within time for the whole life-time of the product. This distribution gives somewhat accurate average estimates in the long term, but it is not able to describe the changes in the hazard rate during the time of operation. Fig. 23 shows the constant hazard rate of the exponential distribution (λ = 100) and the two parameter Weibull distribution (η

= 10 years, $\beta = 4$). The results show that the hazard rate of Weibull distribution exceeds the hazard of exponential distribution after 7.2 years.

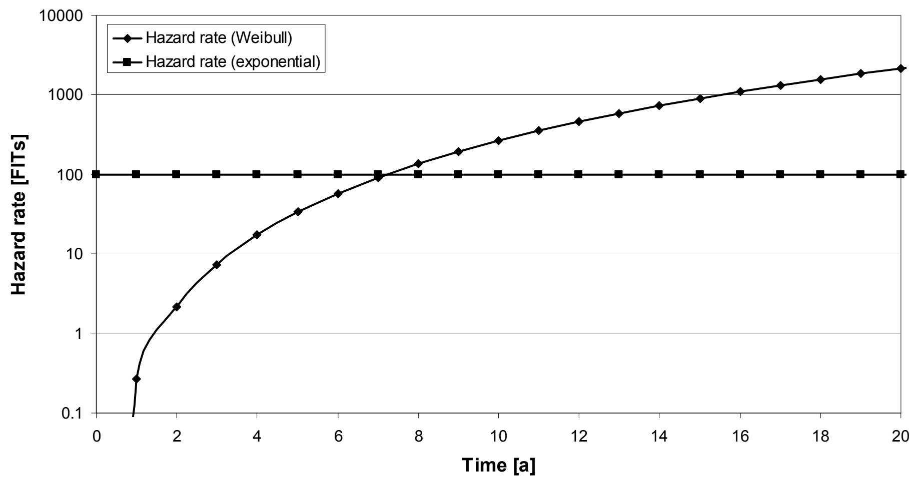

Fig. 23. The hazard rates of the exponential and Weibull distributions, with $\lambda = 100$, $\eta = 10$ and $\beta = 4$. The hazard rate of the Weibull distribution exceeds its counterpart exponential distribution after 7.2 years.

The cumulative distribution function (cdf) of the exponential distribution is

$$F(t) = 1 - e^{-\lambda t}, \tag{26}$$

where t is the time of operation. An example of cumulative failures or cumulative distribution function (cdf), of the exponential and the two-parameter Weibull (per Equation 19) distributions is shown in Fig. 24. The results show that the exponential distribution gives higher cumulative failures during 2.1 years and after this the Weibull distribution will have higher values. As the Weibull distribution tends to more accurately reflect the real field failure distributions, the exponential distribution would give too optimistic values after 2.1 years with the parameters of the given example. For comparison, the cumulative failures of 99.9% are reached after 16 years by the Weibull distribution and after 770 years by the exponential distribution.

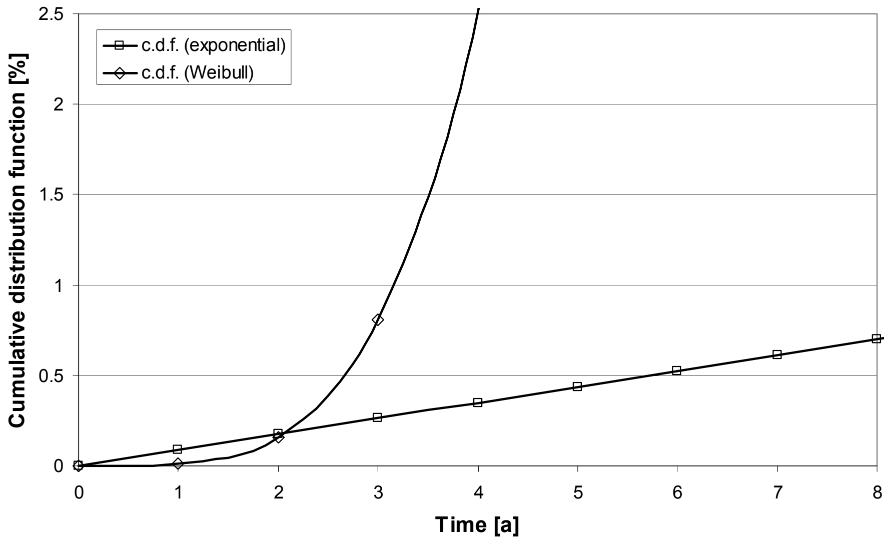

Fig. 24. The cumulative failures per exponential and Weibull distributions. The c.d.f of the Weibull distribution exceeds the exponential distribution after 2 years. β = 4 and λ = 100 were used in the analysis.

Fig. 25 shows two different curvatures of the Weibull distribution, with the same characteristic life η and two different shape parameters, β. This shows that the shape parameter describes the span for the failures. A smaller shape parameter gives wider span for the failure occurrences, which means that there are large deviations within the population under investigation. Ideally, similar products or systems would fail at the same moment in time, which would give infinite value for the shape parameter. So, the Weibull shape parameter can be considered as a factor of material quality and process reproducibility. To conclude, the failure prediction largely depends on the shape parameter of the Weibull distribution (Lall, Islam, Singh, Suhling & Darveaux 2004).

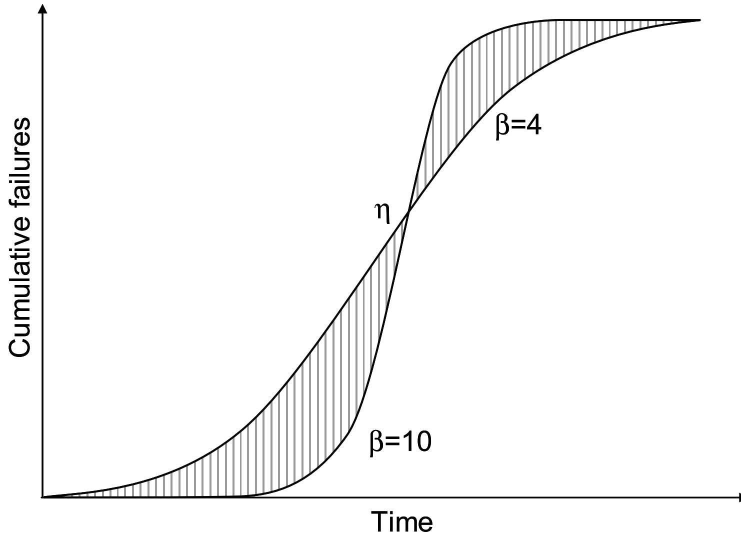

Fig. 25. Cumulative failures as a function of time per Weibull two-parameter distribution. Higher Weibull shape parameter β gives tighter span for the failure occurrence. Both curvatures have the same characteristic life η.

As presented earlier in Fig. 11, the interconnection system consists of the component, the solder joint, the PWB and their environment. Furthermore, the board level design and the product environment establish the stress levels induced in the solder joint system. All the aforementioned qualities have an effect on the lifetime expectancy of the solder joints. Moreover, the component package type and its accelerated stress test characteristics determine the base hazard rate of the interconnection system in the operational conditions. The interconnection Failure-In-Time (iFIT) figure describes the component package specific hazard rate of the solder joints in the given stress conditions. The interconnection FIT figures $h(t)_{SJ}$ can be written as

$$iFIT(t) = h_{SJ}(t) = h_{SJB}(t)\pi_D \pi_E, \tag{27}$$

where $h_{SJB}(t)$, π_D and π_E are the base hazard rate of particular component solder joints, the stress factor of the product design and the stress factor of the environment, respectively. This shows that the interconnection FIT is not constant during the life time. The effect of the time-dependent interconnection failures on the overall product hazard rate is presented in the Fig. 5. Instead of that, the stress factors are considered as constants, which is an idealistic approach for the

stresses. This type of time-independent method has been used with constant base hazard rate by RIAC (2006). In practise the stresses experienced by the products are based on *e.g.* the thermo mechanical history of the solder joints, the power cycles, the thermal management of the product including the solar and other environmental activities affected by the product. An example of the estimated solder joint FITs by RIAC (2006) method is presented in Table 18. The hazard rate λ is calculated by

$$\lambda = \lambda_{SJB}\pi_{SJDT} = \lambda_{SJB}\left(\frac{\Delta T}{44}\right)^{2.26}, \tag{28}$$

where λ_{SJB}, π_{SJDT} and ΔT are the base hazard rate of solder joint, the failure rate multiplier and the solder joint temperature range during one cycle (RIAC 2006:17–19), respectively. The environment is based on the reference by HDPUG (1999), which was also used previously in Chapter 4. The RIAC's method does not take into account the amount of daily cycles for the solder joints, which actually affects the hazard rate of the solder joints. As shown in the Table 18 all the *Plastic IC* packages have the same base solder joint hazard rate, independent from the board level reliability test results or any other property. The interconnection FIT of 2 for *Plastic IC*s would estimate 1 solder joint failure for $5x10^8$ device hours, which in practise can not be true for all the different types of *Plastic ICs*. The hand solder hazard rate could vary from 2.6 to 36.4 FITs depending on the quality and environment factors, MIL-HDBK-217F (1991).

As stated previously, the product failures are estimated by the MTBF predictions; it would be beneficial to take into account the hazard rates of the second level interconnections. The interconnection failures are predicted in the MTBF predictions by using constant hazard rates, which are usually far below the hazard rates used for the components themselves. The typical processor intrinsic FIT is below 100 (Freescale 1999). The time dependency of the interconnection hazard rates is not taken in to account. Salmela *et al.* (2003) published a method of converting time dependent hazard rates in to a form that can be used in the MTBF estimates. In the method, the constant hazard rate values are chosen to correspond for certain time-intervals.

Table 18. The solder joint hazard rates by RIAC (2006) method. The environment categories are by HDPUG (1999). The hand solder figures are by MIL-HDBK-217F (1991).

Component	Base hazard rate [/106] *	Environment Category **	Hazard rate multiplier πSJDT *	Hazard rate, FIT [/109h]
Ceramic Capacitor	0.00095	Installed telecom, ΔT = 45°C	1.0521	1.0
Ceramic Capacitor	0.00095	Portable telecom, ΔT = 30°C	0.4208	0.4
Plastic IC	0.00485	Installed telecom, ΔT = 45°C	1.0521	5.1
Plastic IC	0.00485	Portable telecom, ΔT = 30°C	0.4208	2.0
Hand solder ***	0.0026 ***	1.0–7.0 ***	1.0–20 *** (Quality factor)	2.6–36.4

* RIAC 2006; ** HDPUG 2006; *** MIL-HDBK-217F 1991

Instead of using Equation 27 for the iFIT estimates or the time-independent methods, the following novel approach was chosen in this thesis. After acquiring the test results from the accelerated stress test, the acceleration factor between the stress conditions of the test and actual product is estimated. The accurate estimation involves dividing the actual acceleration factor in to sub-parts. In order to utilize readily calculated values for the actual acceleration factor, standard reference points were set for the accelerated stress test setup, the PWB properties and the stress levels generated by the product thermal design and its operational (environmental) conditions. The reference stress test conditions were chosen in accordance with IPC-9701 TC3, which specifies a thermal cycle from –40 °C to +125 °C with 60 minutes cycle time for component packaging samples mounted on 2.35 mm thick PWB. The reference design utilizes the same aforementioned PWB properties with 5 °C thermal fluctuation once per hour. The reference environment condition was chosen to be *installed telecom* per HDPUG (1999).

The characteristic life in the operational conditions is calculated by multiplying the characteristic life in the test with the corresponding acceleration factor. A mathematical presentation for the method is

$$\eta_{actual} = \eta_{test} \times A.F._{test/actual}, \quad (29)$$

where η_{actual} and η_{test} are the characteristic life for actual product and test population, respectively. The acceleration factor, $A.F._{test/actual}$, between the stresses in the test and in the actual field conditions is

$$A.F._{test/actual} = \frac{N_{test}}{N_{std_test}} \times \frac{N_{PWB_actual}}{N_{PWB_std_test}} \times A.F._{thermal\ \mathrm{design}} \times A.F._{operation_conditions}, \tag{30}$$

N_{test}	Amount of thermal cycles in the test,
N_{std_test}	Amount of thermal cycles in the standard reference test,
N_{PWB_actual}	Amount of thermal cycles for component mounted on the test PWB,
$N_{\mathrm{PWB}_std_test}$	Amount of thermal cycles for component mounted on the standard reference PWB,
$A.F._{thermal\ \mathrm{design}}$	Acceleration factor of thermal design in the actual product and test vehicle (also denoted as design factor, π_D),
$A.F._{operation_conditions}$	Acceleration factor of thermal cycling range in the actual product test vehicle (also denoted as environmental factor, π_E).

The first two multipliers in Equation 30 are needed to estimate the acceleration of the used test setup and its PWB to standard test setup and PWB. The effect of the PWB is commonly neglected from the acceleration factor estimates. The stresses induced to the component solder joints differ between different test setups. When the acceleration to the standard test setup is known, the performance in the standard design and environment can be estimated. These standard hazard rates, or component specific base hazard rates, are then multiplied with the actual design and environment factors for component specific hazard rates in the given stress conditions.

The hazard rate (iFIT) of the component interconnections is calculated from the resulted η_{actual} and the estimated Weibull shape parameter β with the Equation 20 and can be written

$$iFIT(t) = h(t) = \left(\frac{\beta}{(\eta_{actual})^{\beta}} \right) t^{\beta-1}, \tag{31}$$

where t is the time of operation. In this thesis, the intention is to reduce the amount of calculation rounds and to use readily calculated values for the actual hazard rates for the component interconnections. This is performed by estimating first the base hazard rate of the particular component package and then multiplying it by the corresponding acceleration factors. The hazard rate, iFIT, at the standard stress conditions can then be formulated

$$iFIT(t) = \left(\frac{\beta}{\eta_0{}^{\beta}} \right) t^{\beta-1} \times \left(A.F._{0,actual} \right)^{-\beta}, \qquad (32)$$

where η_0 and $A.F._{0,actual}$ are the actual characteristic life of particular component and the acceleration factor between the reference and actual stress conditions. It can be noted that with the milder conditions the amount of thermal cycles to failure will be higher, meaning higher acceleration between the standard and given conditions, and thus, higher $A.F._{0,actual}$. This would result in lower hazard rates. Fig. 26 shows an example of the base hazard rate during the time of operation in log-normal scale. The actual interconnection hazard rate of the particular component in the given stress conditions is obtained by multiplying the base hazard rate with corresponding acceleration factors. The hazard rate in the more severe conditions is higher, so the *severe condition* curve is above the *base hazard rate* curve, Fig. 26.

The actual component specific hazard rate can be obtained by estimating the acceleration factor between the standard conditions and the actual conditions. The advantage of the model is the use of accelerated stress data, which gives a solid basis for the method. The actual stresses are obtained by empirical models, so the whole model is closer to pure empirical than semi-empirical. The advantage of the empirical models is the accuracy when the parameters are changed conservatively.

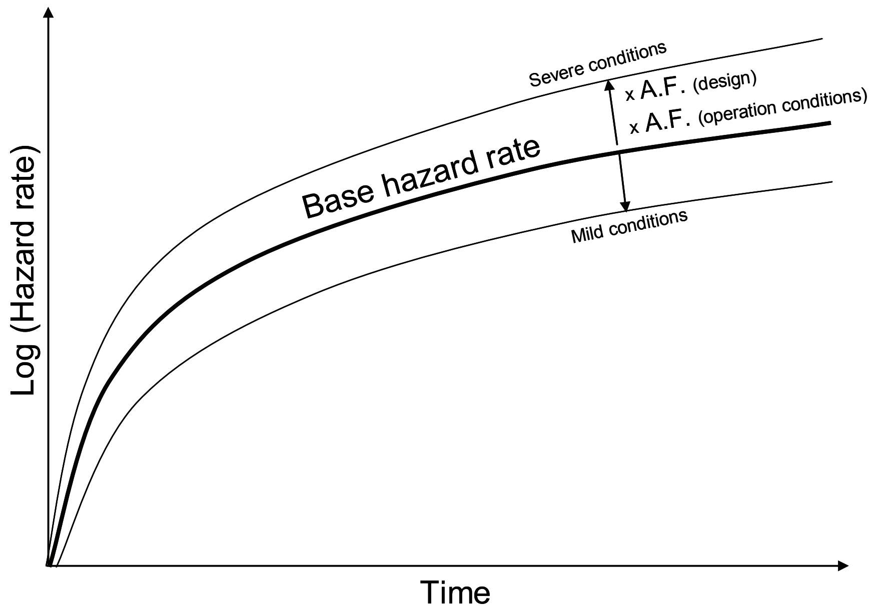

Fig. 26. The base hazard rate of the component interconnections on log-normal scale. The hazard rates in the given operational stress condition are obtained by multiplying the base hazard rate at the given time with the corresponding acceleration factors (A.F.s). Weibull shape parameter of 4 was used in the analysis.

5.2 The base hazard rate of the solder joints

The base hazard rate denotes a hazard rate of the component interconnections in the standard reference stress environment. It could be based on the empirical data (the backwards reliability concept) or could be modelled (the forward reliability concept). The empirical test data is preferred as it gives a solid starting point for the analysis. The disadvantage with the purely model based assessments is the multiple amount of parameters that can not be taken into consideration. In the empirical tests these parameters are built-in in the test specimen and are already solidly in the test results. These parameters include the effect of the PWB surface finish, the effect of the process parameters and the effect of geometrical design of the solder. The base hazard rate also gives a reference measure for the hazard rate estimations of the comparable technologies.

In the analysis, the component packages are categorized to a finite amount of packaging classes. These packaging classes are dealt with as blocks, which have only the measures of *component packaging type* and *normalized stress test result*. The latter denotes the amount of thermal cycles in the standard test conditions. When these figures are known, the analysis utilized readily calculated multipliers for each basic interconnection element to estimate the field performance based on the stress difference analysis. The result of the analysis can be used in the product reliability estimates. In this study, the base hazard rate of the solder joints of a given component is a function of the component package type, the PWB properties, the test specification and the characteristic life in the test.

5.2.1 Package categorisation in the terms of interconnection reliability

The idea behind the field failure estimation method is to understand the solder joint aging mechanisms in thermo mechanical stress conditions. During the temperature fluctuations, the PWB and the component expand and contract at different rates causing a global difference in the material set-up as shown in Fig. 27. There are also local stresses between the solder material, the substrate and the PWB. This expansion/contraction difference induces a stress to the component, the PWB and to their interconnections during the thermal gradients. As the level of the stress is gradually increased, the solder material is usually the first to deform plastically. With the shock loadings, the component substrate or the PWB could be the first to rupture (*e.g.* Mattila *et al.* 2006, Prabhu *et al.* 2000). When the solder joints are deforming during the frequent thermal fluctuations, the mechanical properties of the solder will gradually degrade. This will eventually result in a solder joint failure.

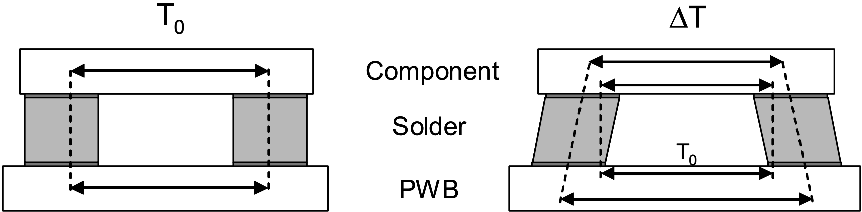

Fig. 27. Schematic presentation of the different thermal expansions during temperature fluctuation.

As the aforementioned qualities are the fundamentals behind the solder joint failures, the only difference between the component packages is their geometrical dimensions. The interfacial phenomena are not a part of this approach. By following this hypothesis, at least three different component package types can be recognised, which are used in this thesis as the main component package categories. These categories are presented in the Fig. 28. Within the leadless packaging types, the *BGA* components have typically the highest stand-off distance. The solder castellated (*leadless)* packages are typically only 10% of that. This means that the "thermo mechanical load-stress-strain" behaviour of the solder joints is remarkably different. The *leaded* components do have a relaxation capability built in the leads, which dramatically reduces the stresses induced to the solder joints. This is why the smaller volume leaded solder joints are far more reliable than the leadless castellated component packages. Despite that, some lead materials are generating very high local stresses due to the material property incompatibility of the solder joint system. For instance, the Coefficient of Thermal Expansion (CTE) mismatch of the NiFe alloys (*e.g.* "alloy-42" and "Kevlar") and the PWB is in the level of 9–18 ppm/°C (Clech, Langerman & Augis 1990).

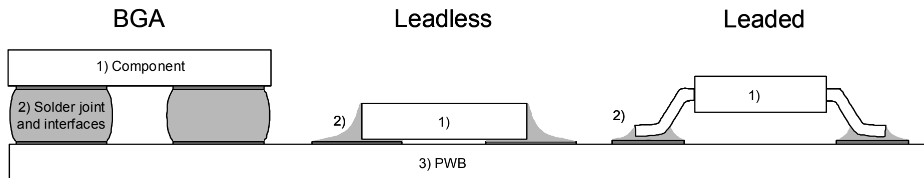

Fig. 28. A schematic presentation of the BGA, the leadless and the leaded interconnection system.

In the component package category based assessment-method the component packages are divided in to several distinct categories. The component package types examined in this thesis are presented in the Table 19. The category is based on the basic set of infrastructure electronics components. Furthermore, the emphasis is in the most critical component packages in terms of the interconnection reliability, included with some typical component package types. The category should be chosen differently for other electronic industry devices, which is not discussed in this thesis. The Ceramic BGA components are not

investigated in this thesis; a comprehensive study of them can be found reference (Perkins 2007).

To conclude, the solder joint volumes and their geometrical dimensions differ between the component packaging types. Also their material properties and sizes differ remarkably from each other. Moreover, the stresses are distributed unevenly within the solder joints and the stress distribution is component specific. With the larger processor components, there are also redundant and non-redundant interconnections, which make the solder joints unequal from the interconnection reliability point of view. Thus, the conventional "constant hazard rate for every component type"-thinking is distorted in the fundamental level. Moreover, there are remarkable deviations in the stress level between the individual solder joints of a component.

Table 19. Categorized component package types used in the thesis and their examples.

Interconnection type	Substrate material	Interconnection media	Packaging examples
Leadless	Plastic	Castellation	Solder castellated laminate substrate
Leadless	Plastic	Bottom terminals	Micro leadframe® *
Leadless	Ceramic	Castellation	Solder castellated ceramic substrate Chip components
BGA	Plastic	Solder balls	Multilayer BT substrate Ball Grid Array
BGA	Ceramic	Solder balls	Multilayer ceramic Ball Grid Array
Leaded	Plastic	Castellation	Thin Small Outline Package

* Amkor 2007

5.2.2 The effect of the test PWB

The material properties of a PWB where the components are mounted do have a major effect on the hazard rates of the solder joints. As stated previously, the PWB is one of the basic elements of the interconnection system, Fig. 11. Syed & Kang (2003) presented that reducing the PWB thickness from 1.6 mm to 0.8 mm the characteristic life in the accelerated stress test increases 47%. This remarkable difference was accomplished only with modifying one parameter of the PWB. To achieve the same level of difference in the test result by modifying the

component, the component packaging should undergo several time-consuming research and development phases. So, the properties of the test PWB must be known accurately, as well as the properties of the end product PWB.

In the category based packaging assessment-method, the test PWB characteristics are compared to the reference test PWB. This is done to enable the usage of readily calculated values in the following steps of the category based assessment-method. Based on the FE modeling (Andersson, Salmela, Särkkä & Tammenmaa 2003) the following relationship between different PWB configurations can be made

$$AF_{PWB} = \frac{N_{test_PWB}}{N_{ref_PWB}}$$
$$AF_{PWB} = \left(\frac{h_{test_PWB}}{h_{ref_PWB}}\right)^{1/6}\left(\frac{E_{test_PWB}}{E_{ref_PWB}}\right)^{1/4}\left(\frac{CTE_{test_PWB}}{CTE_{ref_PWB}}\right)^{5/2}, \quad (33)$$

where *h*, *E* and CTE are the thickness, Young's modulus and the coefficient of thermal expansion of the PWB, respectively. The index *test_PWB* corresponds to the PWB configuration in the particular test and *ref_PWB* denotes the reference PWB configuration. The FE models were done for ceramic BGA component (Andersson *et al.* 2003), with average CTE of 6.25 ppm/°C for the component substrate and 14 – 18 ppm/°C for the PWB. Equation 33 gives accurate estimates at least for the ceramic components. It can be used for plastic components as well, as their CTE is also below the CTE of the PWB. A comparable formula for Equation 33 can be found from the reference (Vandevelde, Gonzales, Beyne, Vandepitte & Baelmans 2004), in where the power figures of thickness, Elastic modulus and CTE relation are from 1.5 to 2.

It should be noted that the variables in Equation 33 are mutually dependent, but for simplicity reasons they are separated in the formula. It can easily be seen that the CTE-relation variable is far more sensitive compared to the height-relation variable. A 1% change in the relation of height, Young's modulus or CTE results in a 0.17%, 0.25% and 2.5% change in the A.F., respectively. A graphical presentation of the required thermal cycles as a function of thickness and CTE of PWB is presented in Fig. 29. 1000 thermal cycles in the test board with a thickness of 2.35 mm and a CTE of 18 ppm/°C was used as a reference. For instance 1400 thermal cycles in a 1.6 mm board with CTE of 16 ppm/°C corresponds to the same level of stress than in the reference PWB.

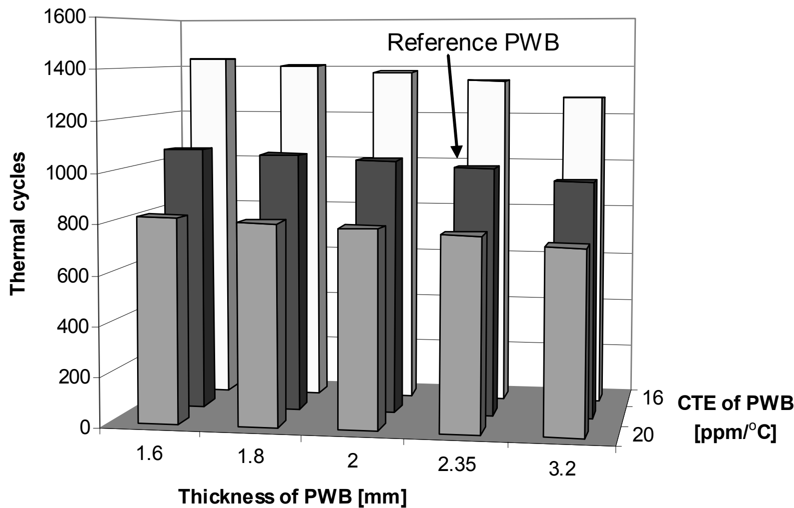

Fig. 29. Graphical presentation of the amount of thermal cycles correspond to the 1000 cycles in the reference test.

The thickness of the PWB itself does not remarkable affect the stress levels of the solder joint system. In practice thicker PWBs have more layers in it, meaning a higher percentage of copper. This affects the Young's modulus and the CTE of the PWB, and in general makes the PWB stiffer. So, all the variables in Equation 33 should be taken into consideration, when the different PWB configurations are compared. Table 20 shows the power of the PWB thickness relation to the thermal cycling performance found from the published data by Syed & Kang (2003), Tee, Ng, Siegel, Bond & Zhong (2004), Texas Instruments (2000) and NECEL (2007a). It can be seen that with the leadless components (QFNs) the height relation is higher than with the BGA packages. This difference might be due to higher CTE and Young's modulus characteristics, as per Equation 33. The power of the height relation to characteristic life of the larger BGAs is closer to the power-figure (*1/6*) used in the Equation 33. This indicates that the Young's modulus and the CTE of the thinner and thicker PWB of the BGA144 and BGA224 components were similar.

Table 20. The PWB height relation to the thermal cycling performance from published experiments.

Component	Measure from thermal cycling test (-40/+125 °C)	Power of height relation to lifetime
QFN 68 *	Weibull η	0.55309
QFN 32 *	1st failure	0.36257
BGA 48 **	Weibull η	0.22545
BGA 144 ***	0.1% extrapolation	0.16912
BGA 224 ****	1st failure	0.16171

* Syed and Kang 2003; ** Tee *et al.* 2004; *** Texas Instruments 2000; **** NECEL Electronics 2007a

5.2.3 The relation of the different accelerated stress test setups

In order to estimate the stress levels of different test setups and their effect on the thermal cycling result, the following formula can be used

$$A.F._{\Delta test} = \frac{N_{test}}{N_{ref_test}} = A.F._{SDNL} \times A.F._{PWB}, \tag{34}$$

where $A.F._{\Delta test}$ is a total acceleration factor between the two test setups, $A.F._{SDNL}$ is a stress dependent Norris-Landzberg relation by Salmela (2007) and $A.F._{\mathrm{PWB}}$ is a stress relation of the different PWB build-ups between the two test setups. The N_{test} denotes the amount of thermal cycles in the test under investigation and N_{ref_test} denotes as the amount of cycles in the standard reference test. The $A.F._{SDNL}$ is written

$$A.F._{SDNL} = \left(\frac{\Delta T_{ref}}{\Delta T_{test}}\right)^{1.9} \left(\frac{f_{test}}{f_{ref}}\right)^{1/3} \frac{\left(A_{s,test} \ln\left(\Delta T_{test}\right) + B_{s,test}\right)^{-\frac{1}{c_{test}}}}{\left(A_{s,ref} \ln\left(\Delta T_{ref}\right) + B_{s,ref}\right)^{-\frac{1}{c_{ref}}}} \times e^{\left[\frac{0.122eV}{k}\left(\frac{1}{Ttest_\max} - \frac{1}{Tref_\max}\right)\right]}, \tag{35}$$

where the fatigue ductility exponents c_{test} and c_{ref} are as per Equation 11 for reference test (*ref)* and the test used (*test)*,respectively (Salmela 2007). In Equation 35, the ΔT, f and $T_{_max}$ are the temperature range during one cycle, frequency of cycles during 24 hours and maximum temperature, respectively. The correction terms (A_s and B_s) are presented in the Table 21. The $A.F._{PWB}$ was described in detail in the previous Section.

Table 21. Correction term parameters for Stress Dependent Norris-Landzberg's model for different materials, Salmela (2007).

Substrate material	Solder	A_s	B_s
Ceramic	Sn37Pb	0.1838	–0.277
Ceramic	Sn3.8Ag0.7Cu	0.0884	0.130
Ceramic	Sn10Pb	0.296	–0.709
Plastic	Sn37Pb	0.299	–0.816
Plastic	Sn3.8Ag0.7Cu	0.179	–0.0953

With Equation 34 the results of different test setups can be converted to correspond the reference test result, so that the base hazard rate of the solder joints could equally be generated. Without this conversion step, the base hazard rate of the interconnections of the particular component would be a function of the stress level of accelerated test. Some examples of Acceleration Factors of different test setups are described in Table 22, calculated using Equation 34. The characteristics of the PWB are presented in Table 23, where the CTE values of 18 ppm/°C and 16 ppm/°C and Young's modulus of 80 Gpa and 15 Gpa were used for the copper and PWB laminate, respectively. The CTE of PWB is calculated by weighting the copper and laminate in their proportion. Equation 34 was developed for the ceramic packages, but it is used here also with the plastic packages due to the relative small difference in the CTE of the PWBs under investigation, Table 23. The –40 °C to +125 °C temperature range with 60 minutes cycle time with components mounted on the 2.35 mm PWB was used as a reference test. The specification of the reference test is per IPC-9701 (2002), with conditions TC3 and NTC-C. The comparison of the stress levels of different tests can easily be made; 1000 hours in the standard test is equal to 3125 hours in the 0 °C to 100 °C test with 30 minutes cycle time. The acceleration factor between the most severe and the mildest test condition is 4.1. This means that there is a remarkable difference depending on what sort of PWB the components are mounted and the conditions in the test chamber. The A.F.s in Table 22 are inline with the previously calculated A.F.s for SnPb solder by Syed (1999), though the thickness of the PWB was not taken into account.

Table 22. The relation of the different test setups on the PWB (FR-4) compared to reference test. SnAgCu solder model was used.

Temperature range		Cycle time	Thickness of PWB	Acceleration to reference test, A.F.(cycles)
Min [°C]	Max [°C]	[Min]	[Mm]	[Cycle/cycle]
–55	+125	60	3.20	1.23
–55	+125	60	2.35	1.14
–55	+125	60	1.60	1.04
–40	+125	60	3.20	1.10
–40 *	+125 *	60 *	2.35 *	1.00 *
–40	+125	60	1.60	0.92
–40	+125	30	2.35	0.81
–40	+125	30	1.60	0.74
0	+100	60	3.20	0.44
0	+100	60	2.35	0.40
0	+100	60	1.60	0.37
0	+100	30	2.35	0.32
0	+100	30	1.60	0.30

* reference conditions in the accelerated stress testing

Table 23. The characteristics of the PWBs.

PWB thickness [mm]	Number of layers	Copper content [%]	CTE [ppm/°C]	Young's modulus [Gpa]
1.6	4	7.5	16.2	19.9
2.35	10	11.5	16.2	22.4
3.2	16	13.1	16.3	23.5

5.2.4 Numerical values for the base hazard rates of component interconnections

The interconnection hazard rate *h(t)* is an expression of the amount of solder joint failures *F(t)* within the population during the time. The hazard rate can be calculated by using the equations of the two-parameter Weibull distribution (Equation 20). In order to estimate the Weibull characteristic life η in reference usage conditions, Equation 10 was utilized with the component parameters presented in Appendix 1 (Tables 48–52). The Weibull shape parameter values of two and four were used for leaded and leadless component types, respectively. The chosen component packaging types were BGA, bottom termination plastic, ceramic leadless, ceramic BGA and copper leaded TSOP due to their different

characteristics of the interconnection system. The component parameters were chosen to correspond to Weibull characteristic life of 400, 500, 700, 1000, 2000 and 5000 thermal cycles (–40 °C to +125 °C 1h cycle) to fit a power law growth. The values are also typical with current component technology (*e.g.* Särkkä *et al.* 2003, Clech 2004 and Syed 2004).

The component interconnection failures in time (iFIT) figures in the *installed telecom*-field conditions are presented in Table 24. The η_0 denotes the characteristic life of a particular component in the standard test conditions. The test results from other test setups must be converted to correspond to the standard test, unless the figures from Table 24 do not apply. The IPC-9701 (2002) recommends using 1000 cycles as a qualification limit for –40 °C to +125 °C test. The components to fulfil this criterion would have hazard rates of 1.5 – 41 after one year of service, depending on the component packaging category.

As shown in Table 24 the hazard rates of the packages with copper leads are under 100 even after 10 years of service whereas the other component packaging types have relatively high hazard rates. This means that the interconnections of the leaded packages are of no concern from the solder joint reliability point of view. The hazard rates for the alloy-42 leaded packages have not been calculated as the effect of the local CTE mismatch is not taken into account in the model used for the hazard rate estimations.

The hazard rate describes the failure occurrence in the given time interval, but it does not however, include the perspective of the amount of total failures. The cumulative failures can be estimated using Equation 19. Table 25 shows the cumulative failures of the different packaging categories in the *installed telecom*-field category. The aforementioned requirement of 1000 thermal cycles means 0.0007% to 59% cumulative failures during 10 years of service, depending on the packaging type. This can not be interpreted from the hazard rate table. So, even fulfilling the required amount of thermal cycles does not guarantee failure free function in the field conditions. This is the fundamental reason why sophisticated tools and methods are needed for solder joint management.

Table 24. Categorized component package types and their base hazard rates (iFIT) per thermal cycle results in the installed telecom-field conditions (ΔT = 45 °C, average 40 °C) at the exact 1, 3, 7 and 10 years. η_0 denotes the characteristic life (63.2%) in reference test conditions and $\eta_{0,f}$ the life expectancy (63.2%) in installed telecom-field conditions.

Component	η_0	$\eta_{0,f}$	iFIT = hazard rate , [1/10^{9}h]			
type	[cycles]	[a]	1st year	3rd year	7th year	10th year
BGA	400	4.6	1100	2.9E+04	3.4E+05	1.1E+06
	500	5.6	480	1.3E+04	1.6E+05	4.8E+05
	700	7.5	150	4000	5.1E+04	1.5E+05
	1000	10	40	1100	1.4E+04	4.0E+04
	2000	19	3.4	91	1200	3400
	5000	44	0.12	3.4	43	130
Ceramic	400	5.8	400	1.1E+04	1.4E+05	4.0E+05
Leadless	500	7.1	180	4800	6.3E+04	1.8E+05
	700	9.6	53	1400	1.8E+04	5.3E+04
	1000	13	15	399	5100	1.5E+04
	2000	25	1.0	32	410	1200
	5000	56	0.05	1.0	16	47
Bottom	400	4.5	1100	2.9E+04	3.7E+05	1.1E+06
termination	500	5.5	490	1.3E+04	1.7E+05	4.9E+05
plastic	700	7.4	150	4000	5.1E+04	1.5E+05
substrate	1000	10	41	1100	1.4E+04	4.1E+04
	2000	19	3.4	92	1200	3400
	5000	43	0.13	3.5	44	130
Ceramic	400	5.8	400	1.1E+04	1.4E+05	4.0E+05
BGA	500	7.1	180	4800	6.1E+04	1.8E+05
	700	9.6	53	1400	1.8E+04	5.3E+04
	1000	13	15	400	5100	1.5E+04
	2000	25	1.2	33	420	1200
	5000	56	0.05	1.2	16	45
Cu-leaded	400	170	7.8	23	55	78
	500	210	5.2	16	37	52
	700	280	2.8	8.5	20	29
	1000	390	1.5	4.5	11	15
	2000	730	0.43	1.3	3.0	4.3
	5000	1700	0.08	0.25	0.57	0.82

Table 25. Cumulative failures of the component package types per thermal cycle results in the installed telecom-field conditions (ΔT = 45 °C, average 40 °C) after 1, 3, 7 and 10 years of service. η_0 denotes the characteristic life (63.2%) in reference test conditions and $\eta_{0,f}$ the life expectancy (63.2%) in installed telecom-field conditions.

Component type	η_0	$\eta_{0,f}$	Cumulative component failures due to interconnection failure [%]			
	[cycles]	[a]	1st year	3rd year	7th year	10th year
BGA	400	4.6	0.23	17	100	100
	500	5.6	0.10	8.1	92	100
	700	7.5	0.03	2.6	54	96
	1000	10	0.01	0.70	19	58
	2000	19	7.4E–04	0.06	1.8	7.1
	5000	44	2.7E–05	2.2E–03	0.07	0.27
Ceramic Leadless	400	5.8	0.09	6.9	88	100
	500	7.1	0.04	3.2	62	98
	700	9.6	0.01	0.93	24	69
	1000	13	3.2E–03	0.26	7.5	28
	2000	25	2.6E–04	0.02	0.62	2.6
	5000	56	1.0E–05	8.3E–04	0.02	0.10
Bottom termination plastic substrate	400	4.5	0.23	17	100	100
	500	5.5	0.11	8.4	93	100
	700	7.4	0.03	2.6	54	96
	1000	10	0.01	0.72	19	59
	2000	19	7.4E–04	0.06	1.8	7.2
	5000	43	2.8E–05	2.3E–03	0.07	0.28
Ceramic BGA	400	5.8	0.09	6.8	88	100
	500	7.1	0.04	3.1	61	98
	700	9.6	0.01	0.94	24	69
	1000	13	3.2E–03	0.26	7.5	28
	2000	25	2.7E–04	0.02	0.64	2.6
	5000	56	1.0E–05	8.1E–04	0.02	0.10
Cu-leaded	400	170	3.4E–05	3.1E–04	1.7E–03	3.4E–03
	500	210	2.3E–05	2.1E–04	1.1E–03	2.3E–03
	700	280	1.2E–05	1.1E–04	6.1E–04	1.2E–03
	1000	390	6.6E–06	5.9E–05	3.2E–04	6.6E–04
	2000	730	1.9E–06	1.7E–05	9.3E–05	1.9E–04
	5000	1700	3.6E–07	3.2E–06	1.8E–05	3.6E–05

Fig. 30 shows the cumulative failures of the BGA components in the *installed telecom*-field conditions as a function of characteristic life in the test conditions (Equation 19). The difference in the performance between the different BGAs can

easily be seen. The characteristic life of 2000 and 5000 cycles are the only ones that have fewer than 10% failure expectation for 10 years life. The interconnection hazard rates are presented in the Fig. 31 for the same aforementioned BGAs. It can be noted that in theory the hazard rate will increase even if the cumulative failure level of 100% has been reached.

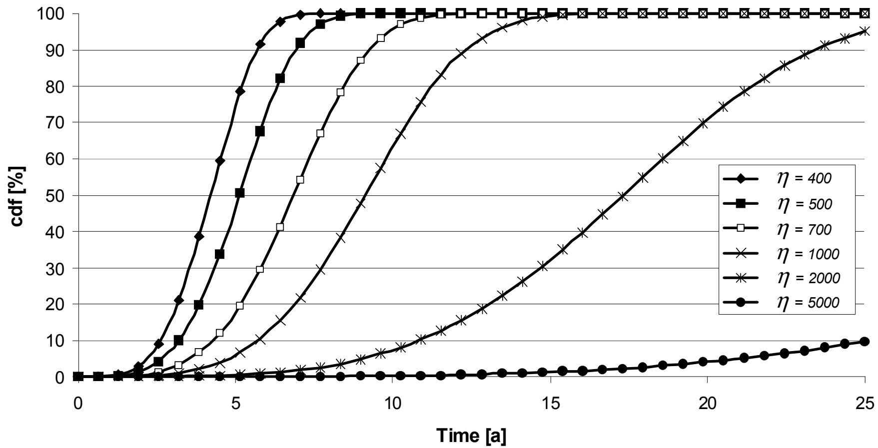

Fig. 30. Cumulative failures of the BGA components in the *installed telecom*-field conditions as a function of the Weibull characteristic life η in the test. Weibull shape parameters of 2 and 4 were used for leaded and leaded interconnections, respectively.

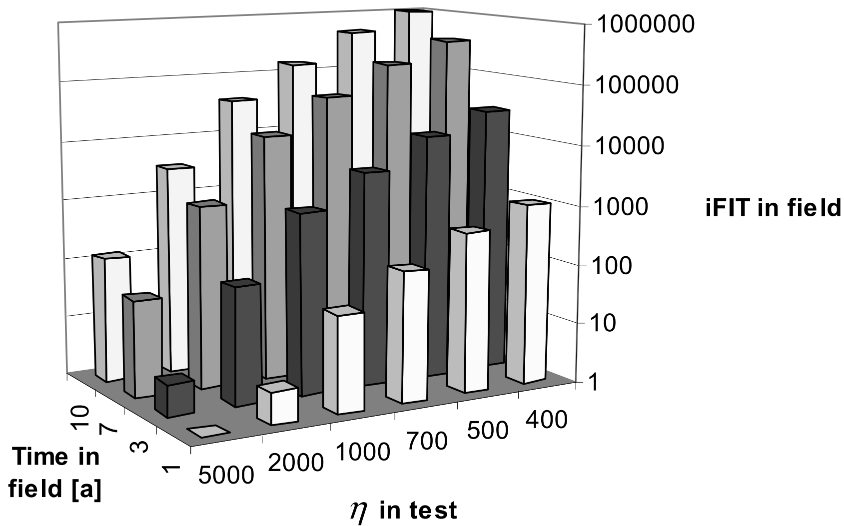

Fig. 31. Logarhytmic chart of the base hazard rate (iFIT) of BGAs in the *installed telecom*-field conditions per Weibull distribution. η denotes to the Weibull characteristic life. For reference, component intrinsic FIT figures are usually below 100 (exponential distribution).

The hazard rate levels in Table 24 are close to the FIT figures used in the earlier solder joint failure assessment methods. The solder joint FIT figure for a leaded component was estimated to be 0.3 for 25 years by Clech *et al.* (1993). The same hazard rate could be estimated with the method in this thesis with 9000 cycles for copper leaded TSOP in –40 °C to +125 °C test and in the *installed telecom*-field category for 25 years. The correlation between the aforementioned methods is thus relatively good.

In the era of mature SnPb Through Hole Technology (THT) and early Surface Mount Technology (SMT) at the beginning of the 1990'ies, the usual accelerated thermal cycling test results for the characteristic life of component interconnections were at level of 10^4 thermal cycles (Syed 1999). This level of hazard rate of such components is close to the Failures-In-Time (FIT) figures used in the earlier solder joint failure assessment methods, when a FIT figure of approximately 1 was used for solder joints (RIAC 2006). Our current solid knowledge of the reliability behaviour of component interconnections is still relying much for the data gathered from the early 1990 products. In spite of the

fact that the methodology and the data have not been reviewed, the technological revolution of components and interconnection media has taken a place. In practise this means that the field failure data is obsolete.

As stated the IPC9701 (2002) specifies 1000 thermal cycles as a qualification limit (for TC3 conditions). By fulfilling this criterion, the components will still fulfil the reliability requirements, at least when proper design and environment is applied. However, with the test results below 1000 thermal cycles, the FIT figure will increase rapidly and high cumulative failures are expected during 10 years of service. With the high demands of reliability within the high stresses, attention to the component selections should thus be paid.

5.3 Conversion factors of the operation conditions

As stated, the stresses induced to the solder joints are generated by temperature changes and by mechanical stresses. There are multiple sources for temperature changes of an electronic product. For example telecom electronics installed to outdoor environment could experience temperature changes due to the environment (*e.g. daily temperature cycle*), due the usage activity (*e.g. Power cycle*) and due to the *thermal management system* of the product. All of these have daily level cyclic and random behaviour. An example of temperature profile of an electronic device is presented in Fig. 32, where the *total* denotes the temperature change seen by the product and its components during one day of operation. The ΔT refers to temperature difference to normal temperature. As the temperature changes are a sum of multiple parameters, the *total* temperature change also has daily variation. To accurately predict the solder joint life time, the stress levels should also be known accurately, together with the other parameters. In reality, the fatigue cycling with constant stress amplitude is rather rare (Klesnil & Lukas 1980: 210).

Instead of using realistic and complex stress models, equalized stress levels are used to describe the cumulative stresses induced to the solder joint during the frequent cycles. The equalized temperature range should be chosen so that the cumulative plastic work is similar to the realistic temperature fluctuation. These standardized stressed per product categories can be found from the references (*e.g.* HDPUG 1999, IPC-9701 2002, MIL-HDBK-217F 1991).

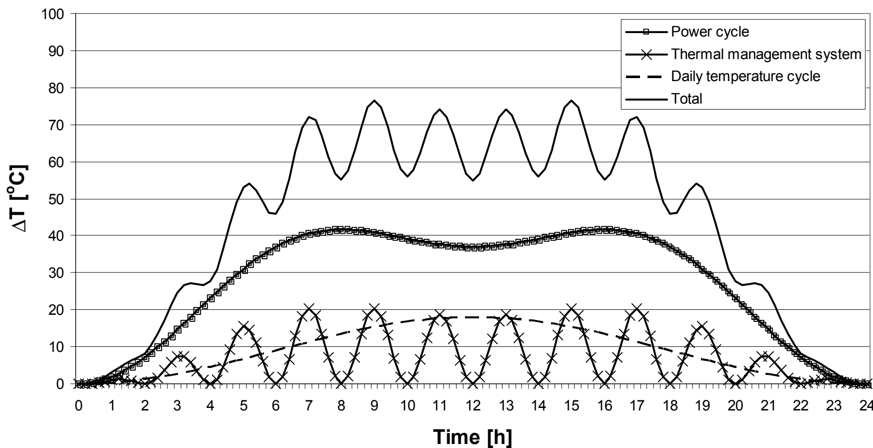

Fig. 32. An example of daily thermal cycle (*ΔT*) experienced by the component solder joints due to the product power cycle, thermal management system (fans) and daily temperature cycle.

In order to obtain the acceleration factors between the different operational or environmental categories the characteristic life for a BGA component in different usage conditions was calculated. Equation 10 was used in estimating the characteristic life of a BGA with 1000 thermal cycles (Appendix 1, Table 50) test performance. Table 26 shows acceleration factors between the standard *installed telecom* and other environmental categories. A higher number means longer life-time expectancy. The comparison of the field categories used in the Chapter 4 is presented in the Table 27. As can be seen, there is a relatively high acceleration between the *installed telecom* and *portable telecom* field categories, which was also concluded in Chapter 4.

An example of cumulative field failures of the above BGA component in the different usage conditions is presented in Fig. 33. As comparison for Table 26, the environmental factors by MIL-HDBK-217F (1991) are presented in Appendix 2. These reference factors are based on the military stress conditions and have values from 1 to 73. It is presented that the A.F. between 165 °C and 50 °C temperature ranges (*ΔT*) is approximately 10 to 13 (Andersson, Salmela, Perttula, Särkkä & Tammenmaa 2005).

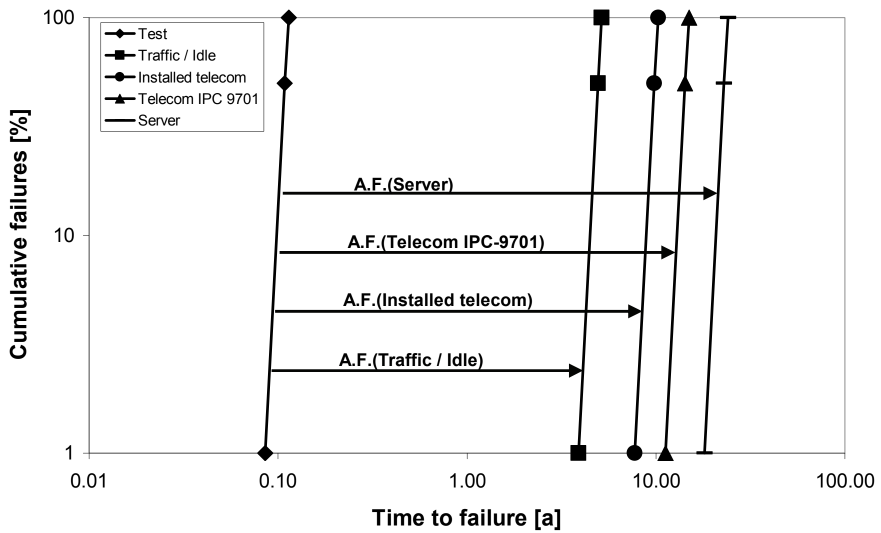

Fig. 33. An example of cumulative failures in the test conditions (line at left hand side) and in the four different usage conditions (HDPUG 1999, IPC9701 2002). A.F.:s describe the acceleration factors between the test and usage conditions.

The results show that the stress conditions of the components in the installed locations have a remarkable effect on the hazard rate of the component interconnections. Also, the operation conditions vary from product to product so that the general level estimations are not accurate for the whole population. Although, when the worst case conditions are known, the first failures can be predicted quite precisely. This information is of great worth during the product maintenance phase, where the first failures can be considered as the initiation point for massive product failures in the whole product population or just the failures of small fraction of population for the most stressed products.

Table 26. Estimated characteristic lives η of a BGA component in the different usage conditions. A.F. denotes the acceleration factor between the different usage conditions.

Standard usage category	ΔT *	η [a]	A.F.
Server. Indoor controlled **	25°C	25.1	2.35
	30°C	19.5	1.82
Telecom ”worst case” ***	35°C	15.6	1.46
	40°C	12.8	1.20
Installed Telecom **	45°C	10.7	1.00
	50°C	9.1	0.85
	55°C	7.9	0.74
	60°C	6.9	0.64
	65°C	6.0	0.56
Traffic / idle	70°C	5.4	0.50

* average temperature of 45 °C and 1 cycle per day; ** HDPUG 1999, *** IPC9701 2002

Table 27. The acceleration factor A.F.(t) between the stresses generated in the different field conditions, also used in the Chapter 4.

Environment device category *	Daily Temperature Fluctuation ΔT *	Cycles Per Day	A.F.(t)
Desktop PC	35 °C	2	0.56
Portable Telecom	30 °C	24	0.23
Installed Telecom	45 °C	1	1.00

* HDPUG 1999

5.4 Conversion factors of the product design

The stresses experienced by the component are different if mounted on the end-product or on the test PWB. The stresses induced to the solder joints of the particular component in the accelerated stress tests are due to the thermal cycling characteristics and the properties of the PWB. In the end-product, the stresses induced to the solder joints are due to thermal characteristics of the product and the material properties of the component, the solder joints and the PWB. So, the differences of the stresses experienced by the solder joints in the accelerated stress test and in the end-product are based on the differences in the aforementioned properties.

The thermal characteristics are based on the daily thermal fluctuations and the power fluctuations of the product. The daily thermal fluctuation is a part of the environment stresses and was discussed in the Section 5.3. The most

important part of the thermal fluctuation experienced by the product is based on the thermal management of the particular components. If the heat generated in the components is effectively dissipated, the thermal fluctuation frequency and its range are minimized. On the other hand, if the thermal design is neglected, components are experiencing multiple high temperature fluctuations during the daily operation.

From the mechanical design perspective, there are differences in the shape and volume of the solder joints between the test and actual PWB. The effect of the different solder land designs and PWB surface finishes should be characterized by testing. The accuracy of the solder joint failure predictions improves if the amount of alternating parameters is minimized. Additional emphasis should also be put on the quality of the component samples. Although, even the measured parameters were identical, they will not produce the same response in accelerated tests (Lall, Islam & Suhling 2003). Table 28 summarizes the differences between the test vehicle and volume product. As stated, the Weibull shape parameter describes the quality and reproducibility of the product population under investigation. The reproducibility of the test vehicles are moderate due to fact that in the manufacturing phase the process parameters are adjusted between the individual assemblies in practise. Also the handling of the components varies lot by lot. Moreover, the manufacturing process of the test component samples and the actual components may differ remarkably. The component samples might come from the uncontrolled process line, whereas the high volume components are manufactured under numerous process control points and test procedures. In product manufacturing, with highly controlled volume production, only minor adjustments are allowed. In conclusion, the Weibull shape parameters from the test do not comply with the Weibull shape parameters of the volume product.

The difference in the end-product PWB and the test PWB has an effect on the hazard rates of the solder joints. By following Equation 33, the stress level comparison of the PWBs can be made. The accelerations between the amount of thermal cycles in the test PWB and actual PWB is shown in the Table 29. Since 0.8 mm thick board has an A.F. value of 1.13 and 3.6 mm thick board 0.88, the thinner PWB has 28% longer life time expectancy.

Table 28. The differences in the properties of the test vehicle and volume product.

Variable	Test vehicle	Volume product
Level of reproducibility	Moderate in the test, but low between the test series	High, but moderate deviation in high population, peak deviations
Component handling	Non-controlled to controlled	Highly controlled
Vehicle	Small series PWB, component specific PWB. Emphasis on the research activities	Controlled volume PWB, design specific PWB (non-component specific)
Assembly process	Partly non-controlled, partly component specific, proto line production	Volume process, under control, compromised parameters
Components	Non-controlled mechanical small series samples with daisy chain connections	High quality, high controlled, high volume components
Interfacial / metallurgical phenomena	Dependent on the daily process conditions, small deviation in component population	Component specific, high similarity in product population, peak deviations
Stress conditions	Highly controlled, monitored, low deviations	Moderately controlled, high deviations
Weibull shape parameter	High	Moderate

Table 29. The acceleration factors (A.F.) for the different PWB thicknesses compared to reference test PWB (2.35 mm).

Thickness / Cu layers	Young's Modulus [Gpa]	CTE [ppm / °C]	A.F.
0.8 mm / 4	24.8	16.30	1.13
1.2 mm / 6	24.2	16.28	1.06
1.6 mm / 6	21.9	16.21	1.05
2.0 mm / 8	22.2	16.22	1.01
2.35 mm / 8	21.1	16.19	1.00
2.8 mm / 12	22.4	16.23	0.95
3.2 mm / 16	23.5	16.26	0.91
3.6 mm / 20	24.4	16.29	0.88

The effect of a frequent low range thermal cycling was estimated using Equation 10 with the BGA component parameters described in Appendix 1 (Table 50). A thermal fluctuation of 5 °C once per hour gives 16 years characteristic life for the BGA components, Table 30. For reference, the characteristic life η in the *installed telecom* field conditions is 10.7 years, Table 26. One should however note that the estimation of the actual effect of the design for the thermal characteristics is a very complex task, and the multipliers from Table 31 should be carefully

considered. As was stated in the previous Section, the equalized stress levels already include certain low range thermal cycling characteristics.

Table 30. Weibull characteristic time to failure in years for BGA solder joints versus the different temperature ranges *ΔT* and the amount of cycles per day (CPD).

ΔT [°C]	Characteristic life [a]			
	12 CPD	24 CPD	48 CPD	96 CPD
5	22.7	15.9	11.4	8.4
10	14.3	9.9	7.0	5.1
15	9.0	6.1	4.3	3.1
20	6.1	4.1	2.8	2.0

Table 31. Acceleration factors A.F. (t) between the different temperature ranges *ΔT* and the installed telecom-field category. The CPD denotes to amount of cycles per day.

ΔT [°C]	A.F. (t)			
	12 CPD	24 CPD	48 CPD	96 CPD
5	0.7	0.6	0.5	0.4
10	0.6	0.5	0.4	0.3
15	0.5	0.4	0.3	0.2
20	0.4	0.3	0.2	0.2

5.5 Validation of the method

Four different components were chosen in validating the method described in the Chapters 4 & 5. The components are a plastic BGA with 1356 Sn37Pb solder joints, a Ceramic BGA with 552 Pb10Sn solder joints, a MLF component with 48 solder attachments (Syed & Kang 2003) and a CLLCC with 10 Sn37Pb solder joints. Test board CTE was 18 ppm / °C, but instead for MLF48 it was 17 ppm / °C. The component parameters are given in Table 54, in the Appendix 1. The accelerated stress test used was –40 °C to +125 °C thermal cycling with 1 hour cycle time, except for the MLF48 it was –55 °C to 125 °C with 30 minutes cycle time. The field conditions were chosen to be 50 °C thermal cycle once per day. All the components were tested by author, except the MLF component (Syed & Kang 2003). ANSYS Mechanical software was used for the FEM modellings.

The results are given in Table 32, with the reference information. The thermal cycle result with the PBGA1356 show very good correlation between the method and the actual thermal cycle result. Anyway, the correlation with FEM predictions is lower. The stress dependent Engelmaier's method, which is the foundation of

the method described in the Chapters 4 & 5, would be expected to give more accurate predictions than the FEM in the lower temperature ranges due to its empirical basis.

A rather good correlation can be found also with the CBGA components, from +15% to +66%. The characteristic life η estimated by the method at the field conditions is very close with the FEM prediction. The MLF48 and the CLLCC10 components have –24% and –12% differences in the characteristic life between the method and the thermal cycling result, respectively. However, the difference to the FEM prediction is relative high.

As conclusion, the method gives a good correlation with the results from the thermal cycling and from the field performance predictions. However, the FEM predictions give more optimistic estimates. This is most probably due to solder model used in FEM, as the difference is rather systematic. Anyway, the empirical background of the model used in this thesis should give more realistic predictions.

Table 32. A comparison of the characteristic life η of four different components made with the method described in this thesis (Chapters 4 & 5) and the reference results. η_{method} denotes to the characteristic life predicted with the model by thesis's method and $\eta_{reference}$ to characteristic life in the references (thermal cycling of FEM prediction). TC denotes to amount of Thermal Cycles.

Component	η_{method}	$\eta_{reference}$	Difference [%]	Method in reference
PBGA1356	706 TC	752 TC	+6.5	Test board thermal cycling
PBGA1356	706 TC	1443	+104	FEM prediction
PBGA1356	11.5 a	18.5 a	+61	FEM prediction
CBGA552	573 TC	789 TC	+37	Test board thermal cycling
CBGA552	573 TC	346 TC	+66	FEM prediction
CBGA552	4.0	4.6 a	+15	FEM prediction
MLF48	5793 TC	5090 TC	–12	Thermal cycling Syed & Kang 2003
CLLCC10	908 TC	735 TC	–24	Test Board thermal cycling
CLLCC10	5 a	9.5 a	+90	FEM prediction

5.6 Tools for component package qualification with respect to interconnection reliability

Instead of using the result of the accelerated stress test as the only qualification criterion for component approval, other approaches could more beneficial from the actual stress condition point of views. For instance, it could be checked

whether the component under investigation is fulfilling the requirements of the high reliability product or whether qualification criteria could be lowered for the components in the milder usage conditions. The standard test or analysis does not answer these questions.

The intention is to find the components and their interconnection media, so that they are as per the product reliability specification, neither under nor over specification. It is obvious, that the components not fulfilling the reliability specification (under specification) should not be chosen. Moreover, the components which are multiple levels above the requirements (over specification) are usually non-beneficial from the component cost point of view or their electrical performance is compromised (could be referred to older packaging technologies). As a conclusion, there is a need for accurate assessment for the board level reliability performance of the component packaging technologies.

In this Section a novel method of assessing the board level performance of the components is presented. Table 33 shows seven measures for component interconnection reliability assessment in the standard design and in the standard environmental stresses. Since the needed methods for *measures 1–7* are described in this thesis earlier, this Section summarizes their usage and their details are not described in detail.

Measure 1 is the conventional "zero failures during 1000 thermal cycles". In here a time to 0.1% failure level was denoted as "failure-free-time". In order to obtain a failure level of maximum 0.1% during the 1000 thermal cycles, the characteristic life of the test population should be at least 2380 thermal cycles. Weibull shape parameter of 8 was chosen; which was based on the multiple accelerated stress test results. The criterion for *measure 1* is simply "passed or failed". The test can be truncated when 1000 cycles with zero failures are reached. This is typically the interpretation of the widely used standard IPC-9701 (condition TC3 and requirement NTC-C).

Measure 2 is another interpretation of IPC-9701 and is closer to the original idea of the requirement specified in the IPC-9701. The test should be conducted at least to the 1000 thermal cycles or to cumulative failure level of 63.2%. *Measure 2* uses a "passed / failed" criterion based on the characteristic life of 1000 thermal cycles, which means cumulative failure of 0.1% in 420 cycles. These two interpretations of the same requirement are actually very dissimilar from the required stress-resistance point of view, and they are still referring to the same standard. Actually, *measures 1* and *2* could be used so that *measure 1* criterion is required from the components in the harsher usage conditions and

measure 2 is a requirement for components intended to be used in the milder conditions.

Measures 3 to *5* are novel methods for component qualification. During the component packaging assessments the cumulative failure levels are estimated in the given field conditions. The time to a certain cumulative failure level is then compared to the reliability requirements of the product. Preferably the stress levels in the real usage conditions should be used in the estimates, but the standard conditions would be a good starting point as well.

Measures 6 and *7* are in-line with the previous three but they give more understanding of the true behaviour of the component interconnections. *Measure 6* described the cumulative failure level during the first three years of operation. Of course the time under investigation can be chosen per product types and their life-time and warranty requirements. *Measure 7* describes the time in the operational conditions, when hazard rate level of 1000 is reached. 1000 FITs was chosen for the limit as after reaching such hazard rate level, the cumulative failures will be growing exponentially.

The intention of the aforementioned methods and measures is to make component packaging technology based qualification assessments and to move away from the one-way-fits-everything kind of thinking. The idea behind this is that component packaging type specific qualification criteria could be used instead of conventional high level generalization. The benefit of such method is to be able to estimate the usage of particular component in the given stress conditions and to avoid over-specification or over-designing.

Table 33. The qualification measures for component packaging technologies from the interconnection reliability point of view. Measures 1 and 2 are commonly used qualification criteria in the infrastructure electronics industry.

Measure number	Description of the measure	Condition / criterion
1	Characteristic life of 2380 cycles in the standard test conditions (0.1% cdf at 1000 cycles, $\beta = 8$) Also known as zero failures during 1000 thermal cycles	Passed / failed
2	Characteristic life of 1000 cycles in the standard test conditions (0.1% cdf at 420 cycles, $\beta = 8$)	Passed / failed
3	Estimated time to 0.1% failure level in the standard design and operational conditions	Time to N_f (0.1%) is compared to the product reliability target
4	Estimated time to 1% failures in the standard design and operational conditions	Time to N_f (1%) is compared to the product reliability target
5	Estimated time to 50% failures in the standard design and operational conditions	Time to N_f (50%) is compared to the product reliability target
6	Cumulative failures at the first three years in the standard design and operational conditions	Amount of failures is compared to the product reliability target
7	Time to 1000 FITs in the standard design and operational conditions	Time to 1000 FITs of the component interconnections are compared to the product reliability target

Table 34 shows an example of the relation of the component packaging qualification *measures 3* to *7* to more conventional *measures 1* and *2*. The conventional test procedure would result only as pass or fail for the specified test criteria, but the *measures 3* to *7* gives more information about the reliability performance in the given field conditions. The time to 0.1% and 1% cumulative failures describes clearly the difference between the requirement specified in the *measure 1* and *2*. The components fulfilling the zero failures during 1000 cycles would have cumulative failures of 0.1% during the 10 years life time. The components fulfilling the characteristic life of 1000 cycles in the test would have the same level of cumulative failures after 4.4 years and 50% during the 10 years. There are thus remarkable differences between the two aforementioned interpretations of the IPC9701.

Table 34. An example of the novel component packaging qualification measures for BGA component. Measures 1 & 2 are compared to measures 3 to 7 in the standard design and operational conditions. Serial numbers from 1. to 7. denote to measures 1 to 7 described in the Table 33. $\beta = 8$.

Test η [h]	Actual η [a]	3. $t_{Nf(0.1\%)}$ [a]	4. $t_{Nf(1\%)}$ [a]	5. $t_{Nf(50\%)}$ [a]	6. F (3 y) [ppm]	7. $t_{h(t)=1000\ FIT}$ [a]
1. 1000	10.4	4.4	5.8	9.9	48	5.5
2. 2380	24.7	10.4	13.9	23.6	0.05	14.8

To compare different component packaging technologies and their failure occurrence under the same conditions the aforementioned analysis was made also to ceramic leadless components (CLLCC*),* shown in Table 35. Thus even having the exact same results in the testing phase, the estimated field performance is better for the CLLCC component. The time to 1% failure is reached within 7.5 years with the CLLCCs, whereas the BGA component reaches same level of failures in 5.8 years.

Table 35. An example of the novel component packaging qualification measures for CLLCC component. Measures 1 & 2 are compared to measures 3 to 7 in the standard design and operational conditions. Serial numbers from 1. to 7. denote to measures 1 to 7 described in Table 33. $\beta = 8$.

Test η [h]	Actual η [a]	3. $t_{Nf(0.1\%)}$ [a]	4. $t_{Nf(1\%)}$ [a]	5. $t_{Nf(50\%)}$ [a]	6. F (3 y) [ppm]	7. $t_{h(t)=1000\ FIT}$ [a]
1. 1000	13.3	5.6	7.5	12.7	6.7	7.3
2. 2380	31.7	13.4	17.8	30.3	0.006	19.7

5.7 An example of the method

To give an example of the method described in Sections 5.1 – 5.4, the following study was made. Let us consider that the usage of a BGA component with characteristic life in the test of 2000 thermal cycles. The test board in this case is a 1.6 mm board and the thermal cycling test setup was 60 minutes cycle time in 0 °C to 100 °C conditions. The product utilizes a 1.6 mm board in the *desktop PC*-environment with usage of additional 5 °C cycle twice per hour by the design. A question could be thus *e.g.* “Should the component be chosen for the product when the warranty time is 2 years, the design life-time is 5 years and 1% failures are accepted during the first 2 years and Weibull distribution with the shape parameter of 4 is expected for the cumulative failure distribution?”

First, Table 24 gives 19 years characteristic life η_0 in the reference conditions for the BGA components with 2000 thermal cycles in the test. However since the test setup was not a standard reference type, the equalized test characteristic life is 2000 × 0.37 = 740 (Table 22) and the η_0 is actually 7.5 years in the standard *installed telecom* field category. By using the Table 27 the A.F. value of 0.56 for the *desktop PC* field category can be found. Additionally the design-A.F. is 1.05 for 1.6 mm PWB (Table 29) and 0.5 for 5 °C thermal fluctuations twice per hour by (Table 31). This results in the actual characteristic life being 7.5 × 0.56 × 1.05 × 0.5 = 2.2 years.

The cumulative failure level of 1% is expected after 0.7 years (2.2 years × 0.32) according to Table 56 from Appendix 3, and thus in this presented example the cumulative failures during the warranty time (2 years) are 50%. This illustrates that the component should be rejected and another component should be evaluated. To fulfil the requirements above, the BGA component should have at least a characteristic life of 5405 thermal cycles in the given test conditions. This value is obtained by choosing $\eta_{0,f}$ = 19 years (Table 24) and calculating the minimum required cycle count in the particular test (Table 22), so 2000 cycles / 0.37 = 5405 cycles. Another way to calculate the needed cycle count is to divide the required 2 years with the estimated 0.7 years and multiplying it with the resulted 2000 cycles in the test, so 2000 cycles × 2 years / 0.7 years = 5717 cycles. More accurate cycle count could be estimated by calculating each sub-phase described in the Chapter 5, instead of using the categorizing as described in this thesis. Anyway, the category based method gives a good idea of the component suitability for the given product and its environment.

5.8 Conclusions

A novel method of interpreting the qualification test data into failure occurrence estimates was presented. The method utilizes the component packaging type specific approach instead of the conventional generic approach. Moreover, the intent of the method is to use readily calculated multipliers in order to estimate the hazard rates of the component interconnections in the given operational conditions. This is made possible by estimating the stress conditions in the test vehicle and in the actual product environment. The method utilizes second level reliability test results for a packaging type specific failure occurrence estimates. Furthermore, the results can be used as such for the component packaging reliability estimates.

The benefit of the method is the ability to compare the different packaging technologies to each other in terms of interconnection reliability in the end-product environments. The advantage compared to the fully modeled (*e.g.* FEM simulation) approach is the utilization of the accelerated stress test data as such. This empirical approach includes the effect of the hidden or background parameters, which are readily in the stress test data.

It was shown that the packaging type has an effect on the hazard rate estimates of the component interconnections. The same characteristic life in the test gives diverge failure occurrence estimates. Also, the effect of the test PWB and the stress conditions must be taken into consideration or the accuracy of the predictions are very poor.

And finally, novel qualification criteria were introduced. Instead of using generic qualification criterion for all of the different component packaging technologies, the component packaging specific criteria should be used. These criteria are intended to describe the true failure behaviour of the component interconnections in the actual operational conditions. The benefit of such a method is to be able to estimate the usage of particular component in the given stress conditions and avoid over-specification or over-designing.

6 Effect of component and SMT process materials on the lifetime expectancy of component interconnections

In this Chapter, the effect of the interconnection and component materials and the solder paste volume variation on the characteristic life of the component interconnections in the usage conditions are introduced and characterized. This includes the type of solder material, the geometrical design of the solder joints and the process variations. The variation of the solder paste volume was chosen for the SMT process related parameter due to its direct effect on the dimensions of the solder joints. The direct influence of the aforementioned qualities to the life time expectancy of the component interconnections is estimated. Usually their influence is assessed only in the accelerated stress test level and they are not interpreted to the real usage conditions. The microstructure and the intermetallic compounds of the solder system also have a remarkable effect on the solder joint ductility and reliability (*e.g.* Wiese *et al.* 2003, Dunford *et al.* 2004, Darveaux 2006), but they are not a part of this study.

One important finding of the thesis is a solder joint defect caused by an excessive component warpage (Fig. 34) during the lead-free reflow due to material incompatibility of Plastic BGA (PBGA). The warpage of the components has been reported to occur in the SnPb process as well (Rao 1997, Yang and Yin 1999), but the magnitude of the warpage in the lead free reflow temperatures is more extensive. In the higher reflow temperatures, *i.e.* in lead-free reflow, short circuits and open circuits have a higher probability to occur. Moreover, a novel method for assessing the range of component warpage in the given process conditions is introduced. By following the method an accurate prediction of the maximum warpage of the PBGAs can be achieved. However, the solder joint defects caused by component warpage might not be detectable during SMT-production and they might cause latent defects in the field.

In this Chapter the effect of the material on the reliability of the solder joints are characterized. Also, a novel method for component warpage estimation is presented.

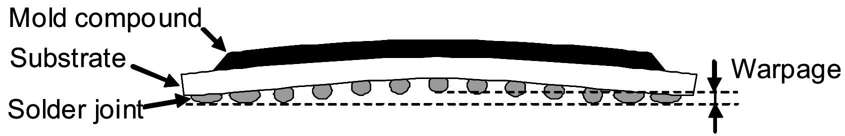

Fig. 34. Schematic illustration of Plastic BGA warpage.

6.1 Effect of the solder material

SnPb solder has been used as a joining material in the modern electronics industry for over than 50 years, where as the new lead-free SnAgCu solder investigations started during 1992 (Clech 2004). The liquidus of Sn4.7Ag1.7Cu ternary eutectic alloy is 217 °C (Hwang 2001: 232) and for its predecessor eutectic Sn37Pb alloy it is 183 °C (Wassink 1994). Due to the higher soldering temperature of the lead-free alloys, the components themselves could be more prone to latent defects after the reflow. The cycles-to-failure, N_f, of the soldering material is a measure of cycle count to 50% load drop with 0.2% strain range (Hwang 2001). The N_f for alloy Sn3.5Ag0.7Cu is 12500 cycles, whereas it is 3650 cycles for Sn37Pb (Hwang 2001: 233). So, from the accounts on the aforementioned cycle amounts, the latter should be more prone to low cycle fatigue.

Also, the PWB and component surface finishing materials have an effect on the properties of the interconnections, but they are not a part of this study. However, their effect on the characteristic life estimates are not neglected completely, as the accelerated stress test results should already contain this information. Moreover, the interfacial reactions between the different joining materials have their effect on the solder joint reliability. Their effect has been investigated in other studies, *e.g.* by Kivilahti (2002), Meilunas and Primavera (2002), Dunford *et al.* (2004) and many others.

The stress-strain behaviour of the solder is dependent on the alloy metals and their compositions. An extensive collection of the stress-strain behaviours can be found from a reference by Hwang 2001. The stress dependency of the fatigue ductility coefficient of SnPb and SnAgCu solders were introduced in detail by Salmela *et al.* (2005). In the study, a natural logarithm was chosen for fitting the experimental measurements, which was also used earlier in this thesis. The natural logarithm gives rather pessimistic estimates for the fatigue ductility coefficient in small temperature ranges, (ΔT <30 °C). This will distort the

characteristic life estimates for components with low cyclic fatigue damage, ΔD, *i.e.* with the BGA-components. In the following, a power function fitting for the plastic component data presented by Salmela *et al.* (2005) is used. The power function formulas of the fatigue ductility coefficient for SnPb and SnAgCu solder materials are presented in Table 36. The component parameters used in the stress dependent Engelmaier model (Equation 10), are shown in Table 37. The results of the analysis are shown in Fig. 35, where the characteristic life of BGA and Ceramic Leadless (CLLCC) components soldered with SnPb or SnAgCu are presented as a function of daily temperature fluctuation range.

The results show that the BGA components soldered with SnPb or SnAgCu should perform similarly in the accelerated stress test, *e.g.* in the –40 °C to +125 °C temperature cycling. The characteristic life ratio is 1.23, with advance of SnAgCu solder. In the milder stress conditions, *e.g.* per *installed telecom*-field conditions (ΔT = 45 °C), the aforementioned multiplier is increased to 2.39. So, the SnAgCu solder gives better performance for the BGA components, at least with daily temperature ranges below 200 °C.

The CLLCC-components have higher cyclic fatigue damage than the BGAs, which gives a different response for the characteristic life versus the daily temperature range. In the test conditions (ΔT = 165 °C) the SnPb solder will have higher characteristic life than the SnAgCu representatives, with ratio of 0.76 for SnAgCu versus SnPb. In the *installed telecom*-field conditions, the characteristic life ratio is 1.26 with advance of SnAgCu solder. In the temperature range of around 70 °C, the SnPb and SnAgCu soldered components will have an equal characteristic life. So, the SnAgCu assemblies will perform relatively better in the milder conditions. Thus using only the accelerated stress test results in the component qualification may lead to pointless rejection of some SnAgCu components (Clech 2004).

Table 36. Fatigue ductility coefficients for SnPb and SnAgCu solder with power function fitting of the temperature range; $x_T = \Delta T$.

Package and solder materials	Fatigue ductility coefficient, $2\varepsilon'_f$
Plastic, SnPb	$f(x_T) = 0.065 x_T^{0.467}$
Plastic, SnAgCu	$f(x_T) = 0.237 x_T^{0.337}$

Table 37. The component parameters used in the stress dependent Engelmaier's model. Unideality factor of 1 was used for both of the components. The values are typical for components used in the infrastructure telecom electronics.

Parameter	BGA	CLLCC
ΔCTE (component – PWB)	4.0 ppm/°C	10 ppm/°C
Solder joint height	0.45 mm	0.20 mm
Solder joint distance	36.8 mm	8.34 mm
	(diag. of 26 mm × 26 mm)	(diag. of 6.5 mm × 10.24 mm)

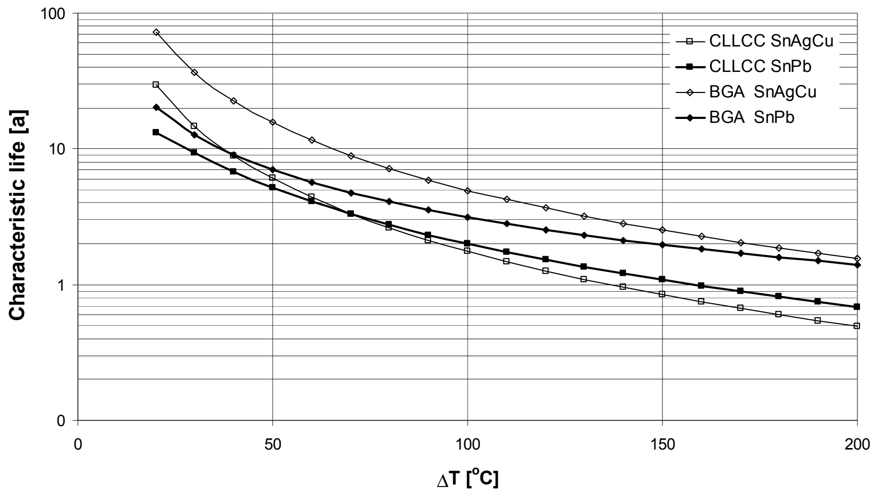

Fig. 35. Characteristic life of BGA and CLLCC components as a function of daily temperature fluctuation. Linear dependency of the temperature range of $2\varepsilon_f'$ was utilized for BGA components and natural logarithm dependency of the temperature range of $2\varepsilon_f'$ for CLLCCs.

Syed (2001) reported a comparison between two test conditions, which were a thermal cycling of 0 °C to 100 °C (TC1) and –40 °C to +125 °C (TC3). The cycle times were 30 minutes and 60 minutes for TC1 and TC3 conditions, respectively. The acceleration factor for the eutectic SnPb solder was 1.96 and 3.21 for Sn4Ag0.5Cu solder alloy (Syed 2001). As a comparison, the stress dependent Engelmaier's model with fatigue ductility coefficients from Table 36 results to acceleration factors of 2.18 for SnPb solder and 3.28 for SnAgCu solder. The component parameters were shown in Table 37. As a conclusion, the power function fitted stress dependent Engelmaier's model show high analogy with the data reported by Syed (2001).

The effect of the solder material on the characteristic life of the solder joints in the accelerated stress test depends on the component type and the used stress conditions. To study the effect of the component type on the solder joint life time expectancy, BGA and CLLCC components were analyzed with the two solders. The characteristic life of the BGA component specified in Table 37 was estimated with the stress dependent Englemaier's model. This resulted in acceleration factors of 1.66 and 1.25 between the characteristic life of SnAgCu and SnPb solder joints for TC1 and TC3 conditions, respectively. Table 38 shows the characteristic life comparisons of different BGA components mounted with SnPb and SnAgCu solder. The acceleration factors between the two solder materials vary remarkably. This might be due to the differences in the cyclic fatigue damage between the different components. The cyclic fatigue damage is also a parameter of stress, which is generated to the solder joints, and has a similar effect as the temperature range has. Also, the die size has an effect on the thermal cycling performance (Gonzalez, Vandevelde , Vanfleteren & Manessis 2005).

Table 38. A comparison of the characteristic life of different BGAs soldered with SnAgCu and SnPb solders.

Source	Component	$\eta_{SnAgCu} / \eta_{SnPb}$	ΔT	Cycle time
Xilinx 2007	BGA 1152	1.08	100 °C	30 min
Xilinx 2007	BGA 676	1.12 [*)]	100 °C	30 min [*]
NECEL 2007c	PBGA 176	2.36	165 °C	40 min
NECEL 2007c	PBGA 385	1.7	165 °C	40 min
Teo 2007	TBGA	2.01	165 °C	60 min
Handwerker 2003	CSP 169	1.67	165 °C	5 min dwell
	CSP 169	2.51	100 °C	5 min dwell

[*] SnAgCu cycle time of 40 minutes was estimated to correspond 30 min cycle time with Equation 35.

The CLLCC components were tested in a temperature cycling test with the TC3 conditions. The size of the CLLCC component was 7 mm × 5.5 mm and it had 12 castellation solder joint on it. The distance to neutral point (DNP) of this quad-type component was 4.5 mm. The PWB had 8 layers and its thickness was 1.8 mm. The cumulative failures are presented in Fig. 36 and the 2-parameter Weibull characteristics are presented in Table 39. The result show that the characteristic life of the Sn3.8Ag0.7Cu soldered components are only 72% of the characteristic life of Sn36Pb2Ag soldered counterparts. The earlier published data shows that the SnAgCu soldered CLLCC-components fail earlier than their SnPb counterparts, Table 40 (Särkkä *et al.* 2004). It can be concluded that a longer DNP

will decrease the Weibull characteristic life ratio ($\eta_{SnAgCu}/\eta_{SnPbAg}$) dramatically. This is due to higher cyclic fatigue damage, ΔD. The result is according to the stress dependent Engelmaier model for CLLCC components. Even the accelerated stress test result is worse for the SnAgCu soldered ceramic leadless components; the estimated life in the milder conditions is higher. In the *installed telecom* field conditions the characteristic life expectation is 26% longer for the SnAgCu than the SnPb soldered components. This is opposite than with the BGA-type of components, explained by higher fatigue damage during one cycle.

Table 39. The Weibull characteristic life η and the shape parameter β of a CLLCC component.

Solder material	η [h]	β	η *(installed telecom)* [a]
Sn36Pb2Ag	703	7.8	6.2
Sn3.8Ag0.7Cu	508 (72%)	5.7	7.8 (126%)

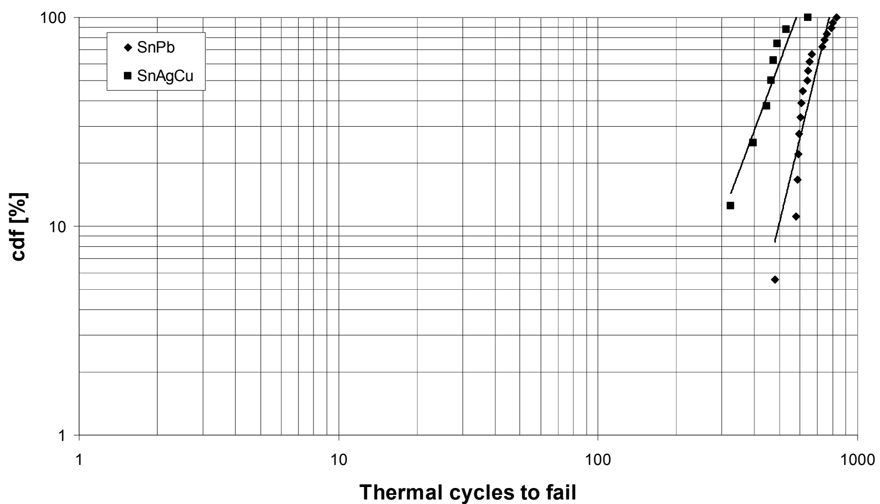

Fig. 36. Cumulative failures (cdf) of the CLLCC component solder joints in the accelerated stress test.

Table 40. The comparison of the SnAgCu and SnPb soldered CLLCCs in the TC3-test conditions (Särkkä et al. 2004). $\Delta\eta$ (SnAgCu/SnPb) denotes the proportion of the Weibull characteristic life of SnAgCu and SnPb soldered CLLCCs.

Component size and its interconnection configuration	$\Delta\eta$ (SnAgCu/SnPb)	Distance to neutral point (DNP)
13.3 × 6.5 Dual-in-line	0.98	4.1 mm
13.3 × 6.5 Quad	0.36	7.4 mm

6.2 Effect of the solder land geometry design

The solder land and the stencil aperture dimensions are one of the key parameters in defining the shape and the volume of the solder joint. These qualities have an effect on solder joint height and its micro sectional area. The height of the solder joint h has an immediate effect to the characteristic life expectancy of the component interconnections, Equations 10, 12 and 13. The shape of the solder joint is a part of defining the level of stress and its distribution in the joint during the thermal cycling. Furthermore, a smaller micro sectional area means shorter path of fracture to be propagated and therefore, shorter time to failure. However before the fracture propagation, a certain stress level is to be reached for the crack initiation. Table 41 shows an effect of a solder land area to the characteristic life of BGA and leadless type of components found from the references.

Table 41. The effect of the solder land area difference (ΔA) on the characteristic life ($\Delta\eta$) of the component interconnections. All the components have non-castellation type of interconnection media.

Reference	Component	$\Delta A_{solder\ land}$	$\Delta\eta$	Notices
Syed & Kang 2003	Leadless	+83%	+92%	Empirical SnPb solder
Tee *et al.* 2004	BGA	+15%	+2.7%	Modelled
Clech 2000	BGA 0.76 mm ball	+19%	+44%	Empirical SnPb solder
Clech 2000	BGA 0.97 mm ball	+19%	+32%	Empirical SnPb solder
Tee *et al.* 2002	Leadless	+20%	+41%	Modelled

The leadless component packages are with or without minimal solder fillets, so that most of the solder is located underneath the component. This is applicable with both BGA and leadless type of components. The results show that when the

area of the solder joint interface is larger, the estimated and measured characteristic life increases. This is due to decreased stress per unit area concentrated to the solder joints and larger area to be fractioned. It can be noted that even a relative small increase in the area of the solder land will increase the lifetime expectancy remarkably. The optimum solder land size from the solder joint reliability point of view of the BGA components is achieved with similar design on the component and PWB side (Zhang, Chee, Maheshwari 2002).

The study of QFN components by Tee (2002) presented that fillet has very minimal effect to the characteristic life. Salmela (2005) presented, on the other hand, that the shape of the solder fillet is one of the most important factors which have an effect on the life time expectancy of the joints. In this Section, the effect of the different solder land areas and solder volumes on the characteristic life of three types of CLLCCs with solder castellation was studied. A Sn3.8Ag0.7Cu lead-free solder was used to study the effect of smaller solder lands or a smaller solder volume. Three CLLCC components with reference solder land geometry and stencil aperture together with a smaller land geometry with reference stencil apertures and reference geometry with a smaller stencil apertures was tested. Fig. 37 shows micro sections of the reference solder land geometry and the smaller solder land geometry. It can be noted that the volume in the solder castellation is greater with the reference land geometry than with the smaller land geometry, so that the length l_1 is greater than the length l_2. On the other hand, the thickness of the solder beneath the component is greater with the smaller land geometry than with the reference geometry, so that $l_3 > l_4$. To conclude, both of the land geometries have its benefits.

The three different CLLCC components with the three combinations of stencil aperture designs and solder land geometry were tested in the –40 °C to +125 °C thermal cycling test with 60 minutes cycle time, Table 42. A total of 90 components were tested altogether. The modifications to the stencil design are from 48% to 89% of the area of the reference design and from 53% to 95% of the area of the reference solder land geometry. Their measured effect on the characteristic life in the thermal cycling test is from 88% to 132%. The solder land geometries were designed so that the smaller solder land area will increase the solder joint height and the smaller stencil apertures will decrease the solder fillet.

The repeatability of the assembly process of the test vehicle has been very high, as the Weibull shape parameter figure is high. The results show that the decreased solder land area will increase the characteristic life of the CLLCC

component solder joints, when the solder volume is kept intact, Table 42. The possible cause for this is the increased height of the solder joint. Also, the characteristic life increase can be explained with the greater solder fillet and with longer path for the fracture. To conclude, the change in solder land area versus the characteristic life of the solder joints has an opposite response with the castellation (CLLCC) and non-castellated (BGA, leadless) interconnections.

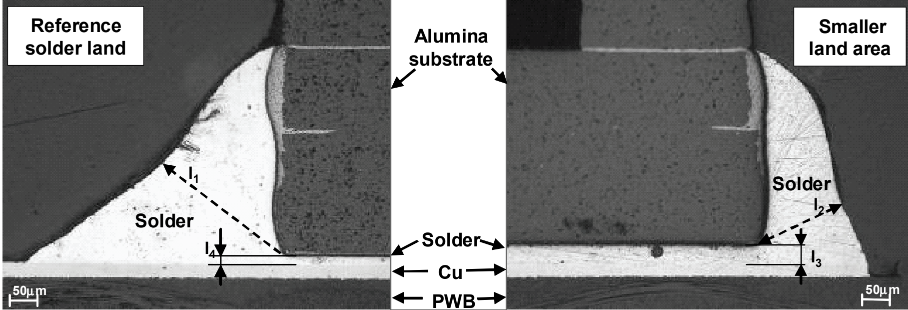

Fig. 37. Micro sections of the solder joints of the reference and the smaller solder land geometry of CLLCC component. The solder thicknesses are denoted as l_1 and l_2. The shortest path for the crack from underneath the component to the surface of the solder is denoted as l_3 and l_4.

The characteristic life of the solder joints of CLLCCs are decreased with the smaller stencil aperture sizes when a smaller amount of solder is applied, Table 42. Also, it will decrease the thickness of the solder fillet. The positive effect of the thicker fillet is then proved. The slightly better performance of the 7 × 5.5 mm^2 CLLCC can be explained with relative wide castellation design in the component, which enables thicker castellation even with the smaller amount of solder.

Table 42. The effect of the solder land and the stencil aperture size on the thermal cycle performance of ceramic leadless packages.

Size of package [mm × mm]	Stencil aperture area standard = 100%	Solder land area standard = 100%	η [cycles]	Ratio	β
9 × 5	100%	100%	407	–	9.9
9 × 5	100%	95%	538	132%	6.7
9 × 5	89%	100%	359	88%	15
13 × 6.5	100%	100%	508	–	12
13 × 6.5	100%	53%	614	121%	11
13 × 6.5	48%	100%	452	89%	11
7 × 5.5	100%	100%	692	–	18
7 × 5.5	100%	88%	902	130%	15
7 × 5.5	86%	100%	709	102%	19

The results of the study confirm that the dimensions of solder castellation have a remarkable effect on the characteristic life of the leadless component solder joints. The higher characteristic life of the smaller land area could be explained with the higher solder joint height and with optimal castellation geometry. This will affect positively to the stress distribution in the solder joint and provides longer path for the crack to propagate.

6.3 Effect of the solder paste volume

Solder paste is the primary source for final interconnection material of most components. In practise only the area array-type of components, where the solder paste brings roughly 10% to 40% of the solder of the final solder joint, differ from this principle. The aforementioned percentages are based on calculations made for common PBGAs with pitches of 0.8 mm to 1.27 mm. For most of the other component package types, the interconnection reliability is based on the amount of solder applied from the solder paste. The volume of the printed solder paste can be expected to follow statistical distributions. A study of one milliard (10^9) solder joints was made by Engelmaier, Ragland & Charette (2000) with automatic X-ray inspection equipment. The study revealed around 0.1% solder joint defect rate, where an open solder joint was found as the most typical root cause. Pan *et al.* (2004) presented that 52–71% of the surface mount technology related defects are caused by the solder paste stencil printing process. In this paper the factors that are affecting the stencil printing process are thoroughly studied. Another aspect for the solder defect rate is the solder joint volume variation, which is

initiated in the paste printing process. The solder joint volume, shape and interfacial reactions are the most important properties in order to achieve reliable solder joints. In this Section the effect of the solder volume on the board level reliability is estimated.

The solder paste printing repeatability was investigated in order to estimate its effect on the solder joint reliability. The tests were conducted with 0.4 mm pitch TSSOP56 components with 120 µm and 150 µm thick stencils. Squeegee angles of 45° and 60° were used for type 3 Sn3.8Ag0.7Cu solder paste. A total of 32 boards and 1792 solder paste deposits were measured with automatic optical measuring system. The theoretical and measured volume of the printed solder paste deposits are presented in Table 43. The measured volume with the 120 µm thick stencil is closer to the theoretical value than with the 150 µm stencil. This is due to the more optimal ratio of aperture size to stencil thickness. Commonly used process limit for type 3 solder pastes for stencil aperture area to wall area ratio is 0.66 or higher (*e.g.* Pan *et al.* 2004; Belmonte, Shah, Jensen & Lasky 2007). The area aspect ratio is higher with the thinner stencil (120 µm) and its solder paste transfer efficiency is higher (98.6%), Table 43. The squeegee angle did not have a noticeable effect on the solder volume.

Table 43. Solder paste printing efficiency of 120 µm and 150 µm thick stencils.

Stencil thickness	Theoretical volume	Measured average volume	Transfer efficiency	Stencil aperture aspect ratio
120 µm	28.3×10^{-3} mm^3	27.9×10^{-3} mm^3	98.6%	0.79
150 µm	35.4×10^{-3} mm^3	31.7×10^{-3} mm^3	89.5%	0.63

The standard deviation in the solder volume is 9.5% when printed with the 120 µm stencil and 11.7% with the 150 µm stencil, Table 44. In this study, it is assumed that 50% of the solder paste is metallic solder. Also it is expected that the height of solder joint will deviate in third root of a standard deviation of the maximum volume. This would result in ±3.07% and ±3.75% deviation in solder height for 120 µm and 150 µm stencil thicknesses, respectively. The solder paste volume distributions of both stencil thicknesses are presented in Fig. 38. As can be seen, the curvatures are overlapping. A relative high proportion of the measured solder paste depositions printed with 150 µm stencil are below the volume of the 120 µm stencil.

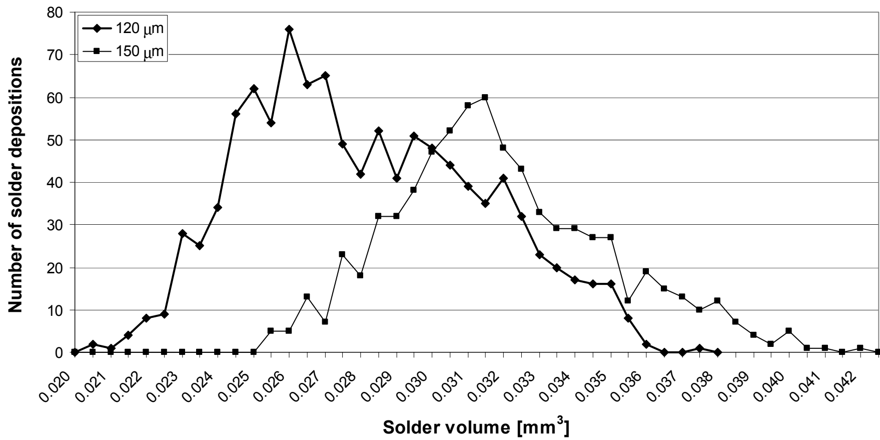

Fig. 38. The distribution of solder paste volume, printed with 120 μm and 150 μm thick stencils. A total of 1792 deposits were measured.

Table 44. A volume deviation of the solder paste deposits of a TSSOP56 component with 0.4 mm lead pitch.

Stencil thickness	Number of boards	Number of solder joints	Standard deviation of volume	Min / max
120 μm	13	728	9.5%	60%
150 μm	19	1064	11.7%	54%

To estimate the effect of the solder volume on the joint reliability, the characteristic life of a CLLCC component was modelled by using the method presented in Chapter 4. The ceramic leadless package was chosen due it being more prone to solder fatigue than the leaded TSSOP. The same solder volume deviations are used as with the previous TSSOP component study, ±3.07% and ±3.75%, with solder joint height difference of ±1.0% and ±1.2%, respectively. The effective solder joint height of 200 μm was used as a reference. The characteristic life of the SnAgCu and the SnPb soldered CLLCC components as a function of solder joint height difference is shown in Fig. 39. The estimated characteristic life varies from 6.1 years to 6.4 years with the SnPb solder and from 7.6 years to 8.0 years with the SnAgCu solder.

To estimate the sensitiveness of the solder paste volume deviation on the characteristic life of the interconnections, two different types of component packages were compared to each other. A CLLCC and a BGA type of component

were chosen for the study. The stand off height of the BGA component is less dependent on the applied solder paste as solder is already attached to the bottom of the component. For the BGA analysis, solder ratio of 1:3 (solder from the solder paste to the solder from the BGA balls) was used. The CLLCC components are more sensitive to the solder volume deviation, due to all of the solder is being initiated from the solder paste. Also the CTE mismatch between the CLLCC component and the PWB is higher. These two component types should represent the extremes from the solder volume sensitiveness point of view. 200 μm effective solder joint thickness was used for the CLLCC component and 450 μm stand off for the BGA-component. A deviation of ±10% in the applied solder volume was compared to the reference applied solder volume. This is a pessimistic approach, but it gives a relative difference in the characteristic life of the chosen component packages. It is assumed that the solder height is deviated with third root of the solder volume deviation. This results to 1.1% deviation of the solder joint height of the BGA and 3.2% for the solder joint height of the CLLCC.

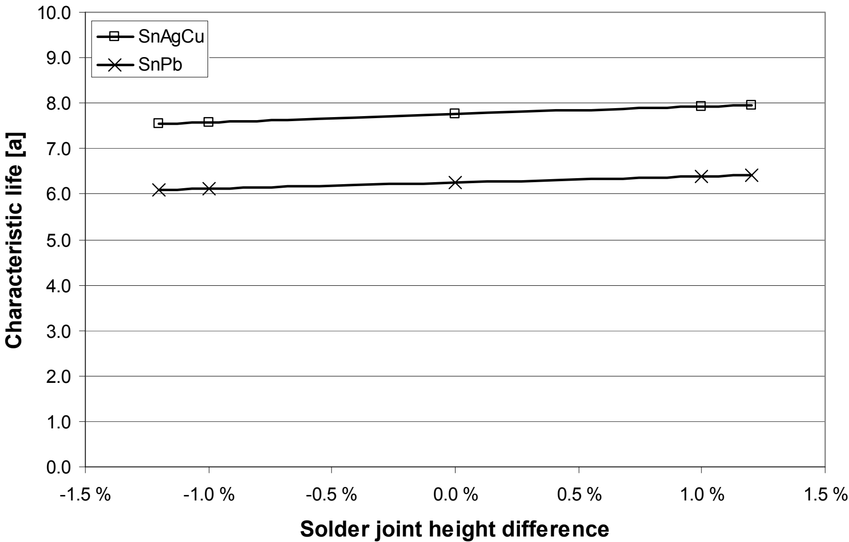

Fig. 39. The characteristic life of a CLLCC component as a function of solder joint height difference.

The effect of the solder joint volume deviation on the estimated characteristic life is presented in Fig. 40. The characteristic life deviates from –7.1% to 6.6% and from –2.5% to 2.4% for CLLCC and BGA components, respectively. It can be noted that the relative characteristic life of the BGA is equally sensitive for the solder joint height, as the curves are parallel. The minor difference in the characteristic life is due to the minor dependence of the applied solder.

To study the sensitiveness of the solder joint height on the characteristic life estimates, the modified Engelmaier's model was used due to its empirical background, presented in detail in the Section 4.1. The acceleration factor, $A.F._{height}$, for two different height parameters h can be written

$$A.F._{height} = \frac{N_{h1}}{N_{h2}} = \left(\frac{\Delta D_{h1}}{\Delta D_{h2}}\right)^{1/c} = \left(\frac{h_2}{h_1}\right)^{1/c}, \tag{36}$$

where N_{h1} and N_{h2} are the number of cycles to failure for solder joint heights h_1 and h_2, respectively, and c is the fatigue ductility exponent described in the Section 4.1, Equation 11. It can be concluded from Equation 36 that higher joints will result in more cycles to failure (as parameter c can get only negative values). So, based on the empirical data, higher solder joint result in higher characteristic life. The $A.F._{height}$ is not only a function of the ratio of the solder joint heights, h_1 and h_2, but as well a function of the mean cyclic solder joint temperature, T_{SJ}, and half cycle dwell time, t_D. This means that the component type itself does not have an effect on the sensitiveness of the solder joint height to characteristic life. However, the component package type, or more precisely its solder land geometry does have an effect to the volume of the applied solder paste versus solder joint height as was shown in the Section 6.2. The variation of the solder volume has a lesser effect on the characteristic life than the solder land geometry design. The effect is typically under 10%, whereas the solder land geometry is tens of percentages.

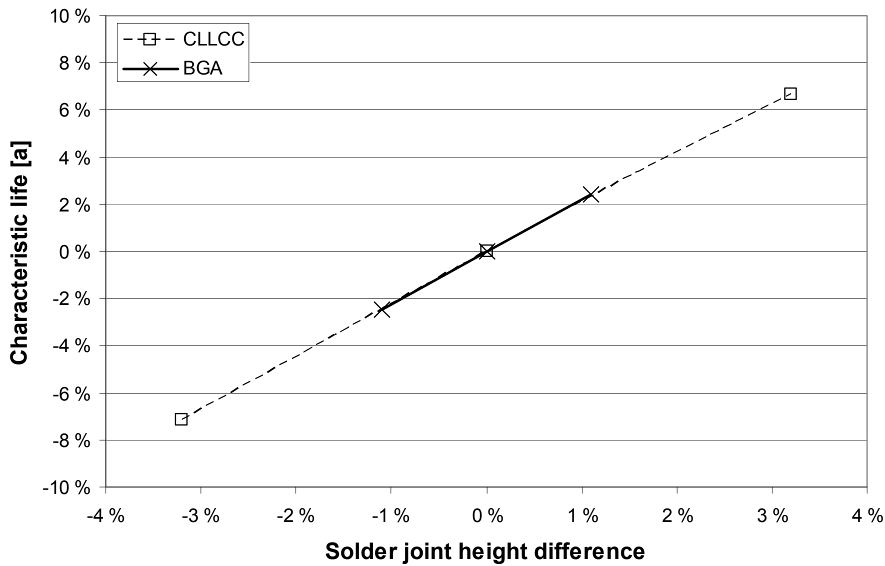

Fig. 40. The effect of the variation of the applied solder volume (±10%) on the characteristic life of CLLCC and BGA components.

6.4 Effect of component material incompatibility in lead-free reflow – BGA warpage phenomenon

A novel defect mechanism of the solder joints of a Plastic BGA (PBGA) component has been revealed. The solder joint defect caused by an excessive component warpage is considered a random failure, but by the nature of its symptom, it can be taken as a systematic failure. However, its effect on the solder joint reliability is not known and can not be predicted accurately. The solder joint defects caused by component warpage can be avoided with proper component material selection (Chien, Zhang, Rector & Todd 2007) or by adjusting soldering temperatures. The latter might need component specific adjustments, which is usually a very limited option. This is due to the SMT process soldering temperatures that are dependent on the solder material in use and the board assembly configuration.

Warpage of a component could be defined as a difference in height between the highest and the lowest point of the component package with respect to the

seating plane. It is a temperature dependent bending of a component package. The warpage is to be distinguished from the coplanarity, which is a maximum distance from an individual solder ball to the seating plane at room temperature (Särkkä, Rahko, Nieminen & Tammenmaa 2006). It has been presented that a coplanarity of 150–200 μm does not itself have a negative impact on the solder joint reliability of SnPb soldered PBGA components with pitches of 1.27–1.5 mm (Huang & Chu 1998).

An excessive warpage of a PBGA component will result in an additional compressive force to the solder joints in the corners of the component. The surface tension of the solder balls in the middle of the component package, where the component stand off tends to increase locally will increase the compressive force in the solder balls in the corners. The surface tension together with the gravitational force of the component will decrease the solder ball height in the corners (above liquidus temperature). As a result of this, and with the fact that the solder volume remains the same, the maximum diameter in horizontal (x- and y-) directions will increase, Fig. 41. At the certain compressive force the adjacent solder balls will get in contact and might get wetted from each other, and end up as short circuits, Fig. 42.

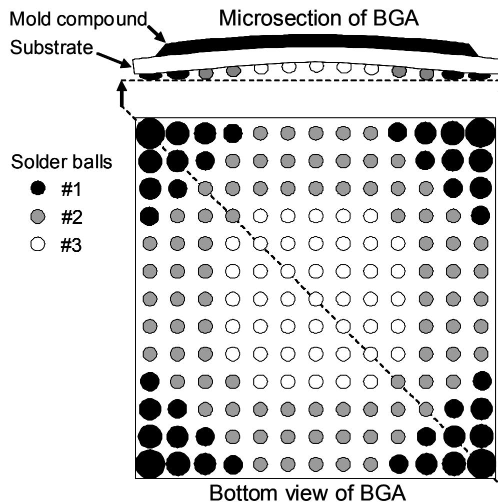

Fig. 41. A schematic presentation of a BGA component and the categorization of the solder ball types, #1–#3. When the component warps during the reflow, the solder balls in the corner (#1) of the component are of danger to short circuiting. In the other hand, the solder balls in the middle (#3) have high probability for opens.

If the compressive force is lower, for instance with the BGA components with periphery solder ball configuration or with lighter weight, there is not enough force to short-circuit the corner balls. As a result of this and together with an excessive warpage, the inner row solder balls will not get in contact with the solder on the PWB and no connection is generated as shown in Fig. 42. This novel solder joint defect might not be detectable during the SMT process.

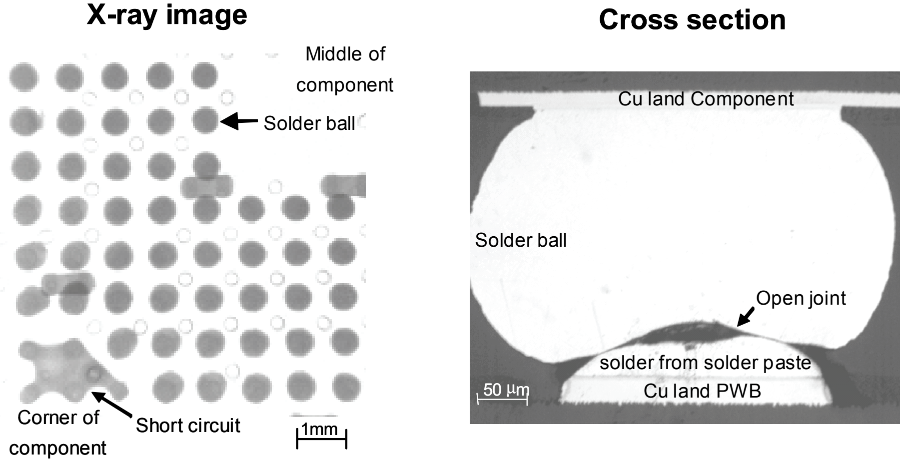

Fig. 42. Soldering defects caused by BGA warpage. Left: an x-ray image of short circuited solder balls in the corner of BGA. Right: an open solder joint in the middle row of a BGA.

In the schematic presentation of Fig. 41, the solder balls labelled as *#1* are in danger of short circuiting, whereas the *#3* solder balls might suffer from opens. The *#2* solder balls are in the low-danger zone and not usually experiencing short-circuits or opens. The actual width of the low-danger zone depends on the solder ball diameter, the pitch, the amount of the solder balls and their distribution and many other minor parameters. Also the ingressed moisture into the PBGA increases the amount of warpage (Vaccaro, Shook, Thomas, Gilbert, Horvath, Dairo & Libricz 2004) and the curing time of the mold compound has it own effect on the range of warpage (Wu, Shiue, Wu, Hung & Lee 1999). The warpage of the component is temperature dependent, so the amount and the warpage vary during the reflow. The orientation of the warpage can vary from concave to convex during the reflow (Shook, Gilbert, Thomas, Vaccaro, Dairo, Horvath, Libricz, Crouthamel & Geriach 2003).

To understand the basic reason for the open solder joint defects caused by excessive warpage the behavior of different materials during the reflow was investigated. These include the solder paste and the PBGA warpage as a function of temperature. In principle, the solder paste consists of a flux system and the solder metal particles (Wassink 1994). The amount of flux is usually in the level of 50% in volume (Wassink & Verguld 1995). The ingredients of the flux are designated to remove contaminations and to reduce the metal oxides and to prevent the additional oxidation prior to soldering. The reducing reaction between the flux activator and the metal oxides enables to expose a clean metal surface. The volatile contents of the flux evaporate prior to the peak temperature in reflow, when it is not usually needed anymore. The solder paste volume decreases during the pre-heating phase of reflow, so that up to 50% of its volume is decreased after the flux evaporation. An example of the component warpage as a function of reflow temperature is presented in Fig. 43. The maximum warpage is estimated for the center solder ball of the PBGA. The decreasing of the solder paste thickness during the reflow is also presented. During the pre-heating phase of the reflow the component is first experiencing a concave warpage and shortly after that it turns to a convex warpage orientation.

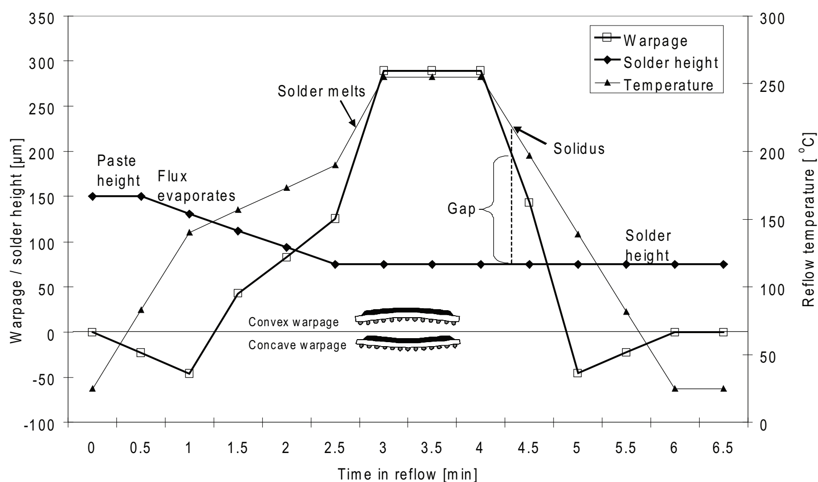

Fig. 43. An example of a PBGA component warpage as a function of the reflow temperature, estimated for the solder ball in the middle of the component. In the time of the solder solidification, the warpage of the component is higher than the applied solder (*Gap*). This means that the solder from the solder paste and solder from the PBGA do not mix and their joint will be inconsistent after the solidification.

It can be noted that when the liquidus temperature (217 °C) is reached, there is a gap between the solder paste deposited on the PWB pad and the solder ball attached to the PBGA. The gap even enlarges when the reflow peak temperature (240–260 °C) is reached. During the time when the solder is above the liquidus, the surface of the Sn-rich solder oxidizes to stannous oxide (SnO) and to stannic oxide (SnO_2) at fast rate. At the temperature of 250 °C, Sn oxidizes even with the extremely low partial pressure of oxygen (Kuhmann, Preuss, Adolphi, Maly, Wirth, Oesterle, Pittroff, Weyer & Fanciulli 1997). The wetting ability of the SnAgCu solder to the tin oxides is known to be poor, even with the active fluxes. So, if the oxide layers on both solder surfaces are not physically broken, the mixing of solder will not happen. Moreover, as all of the flux activity has already been used prior the peak reflow temperature, the mixing of the solder in the PWB pad and in the PBGA solder ball are improbable.

During the cooling phase of the reflow, the solders in the PWB pad and in the PBGA solidificates but the gap between them still remains, Fig. 43. At the temperature of 180 °C the solders are finally getting to contact, but as they both have already been solidified, a continuous solder joint will not form between the interfaces of PWB and the component. As there is no connection during the time when the solders are liquid, their interconnection will not be uniform, or there is no interconnection at all, Fig. 42. The mechanical and electrical properties of such interconnection are very poor. The oxide layers in the surface of the mechanically contacted SnAgCu solders will deteriorate the signal integrity (Burlacu, Nguyen & Kivilahti 2005). Moreover, this sort of open solder joint might have a mechanical contact and it might work as a part of signal path during the product testing and verification phases. So, the failure is randomly detected during manufacturing and it causes early failures in the field.

When the temperature decreases from reflow peak temperature to 150 °C, the component warpage orientation turns from convex to concave. So, the component forces its solder balls against the solder in the PWB. If this was to happen with the temperature of close to solidus, the solders might still be wetted. Anyway, the mechanical structure has been settled when the solder has solidified, meaning that convex warpage of 200 µm will remain. The component and its interconnections are experiencing high stresses during the cooling phase of reflow, as the component attempts still to form a concave warpage of 50 µm at 150 °C. Such stresses can cause cracking inside the component and result in open signal paths in the copper traces (Moore & Javis 2000).

6.5 Novel method to estimate the maximum warpage of a plastic BGA

The method and the formula of a warpage estimation presented in this Section is a further development from the publication by the author (Särkkä *et al.* 2006). The model utilizes a straightforward mathematical approach for a geometrical distortion of a jointed bi-material structure. Such a method was not found in the literature survey. The model gives an accurate prediction of the maximum warpage of a PBGA component. Actually, the accurate value for the warpage is only a secondary target. The primary target is to understand the behaviour of the PBGA component during the lead free reflow and to help to solve possible defect cases, in which the method is found to be very useful. The method is limited to the PBGA components, or any other bi-material components, which have an elastic rubbery state of the materials above 100 °C.

The effect of the die is excluded from the formulas, which might distort the accuracy of the obtained maximum warpage, especially with larger die sizes. With the smaller die sizes, which are typical for PBGAs, the method should be applicable enough. Fig. 44 shows warpage tests done for 37.5 × 37.5 mm^2 size PBGA components with different die sizes (Vaccaro *et al.* 2004). In this thesis, a mold compound dimension of 36 × 36 mm^2 was used for die to package area ratio calculations. The effect of the die size under 10% has a relative small impact to the maximum warpage, if the no-die situation is excluded. Research made from data published by world wide component manufacturer showed the die to substrate area ratios of 3% to 30%, (NECEL 2007b).

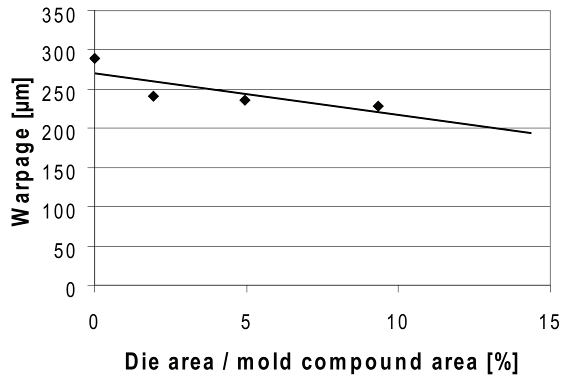

Fig. 44. A maximum measured warpage of 37.5 × 37.5 mm^2 BGA as a function of die versus mold compound area ratio (data by Vaccaro *et al.* 2004). The ratio calculation was done for 36 × 36 mm^2 mold compound area.

In the following, the intermediate stages to proof the formula for the warpage estimation is presented. The PBGA package consists of two planar materials with different material properties; a mold compound, attached to a substrate. The mold compound consists of epoxy resin with filler particles and additional ingredients (Yang & Yin 1999), which adjust the material properties (Darveaux, Norton & Carney 1995). The substrate material consists of laminate made of an epoxy resin, which is reinforced with glass fibers. It is expected that the lengths of the mold compound, $l_{0,MC}$, and the substrate, $l_{0,S}$, are equal at room temperature (25 °C), Fig. 45. The lengths $l_{0,MC}$ and $l_{0,S}$ should be chosen by the side dimension of the mold compound instead of diagonal length. This might be an optimistic approach but it compensates the effect of the die. The distance between the centers of these two combined materials are denoted with $t_{c\text{-}c}$.

In general, the increase in linear dimensions, l, of a solid material resulted from a change in temperature is calculated by

$$l = l_0 \left(1 + \alpha \Delta T\right), \tag{37}$$

where l_0, α and ΔT are the initial length, the coefficient of thermal expansion (CTE) and the temperature change of the material, respectively (MAOL 1978). The change in length is denoted as Δl_{MC} and Δl_S, for *the mold compound* and for *the substrate*, respectively, Fig. 45. As the two materials have different thermal expansions, the changes in length during the temperature changes are not equal.

So, the length difference of *the mold compound* and *the substrate* depends on their temperature. When these materials are bound together and they are expected to be flexible enough, the joint bi-material system will be bent, known as warpage. A spherical form is expected for the bent homogenous materials, so that the radius of curvature *r* is constant through the component in the given temperature. Fig. 45 shows an example of bent bi-material system in elevated temperature.

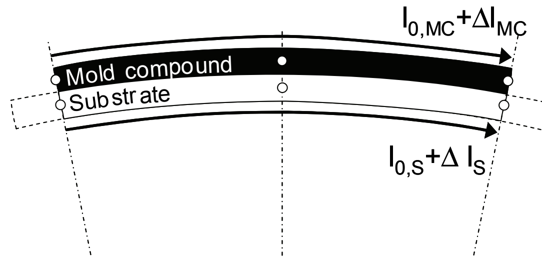

Fig. 45. Warpage of the mold compound and the substrate as a result of different thermal expansions.

The CTE of the materials is temperature dependent. During the reflow, especially the plastic materials can experience two different CTEs; one CTE below and another CTE above the glass transition temperature. The glass transition temperature is defined as “the temperature at which an amorphous polymer, or the amorphous regions in a partially-crystalline polymer, changes from being in a hard and relatively-brittle condition to being in a viscous or rubbery condition” (IPC-T-50G 2003). Fig. 46 shows an example of the CTE of a plastic material in below and above the glass transition temperature, T_g.

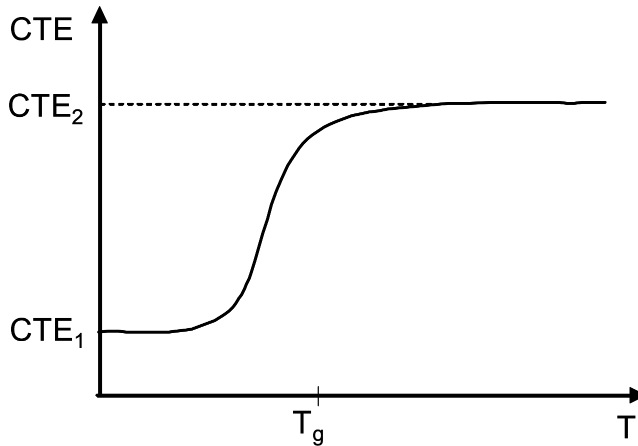

Fig. 46. An example of the CTE of an epoxy resin material as a function of temperature.

The glass fibre reinforcements control the thermal expansion of the substrate material. Thus, the CTE of the substrate is relatively independent of the temperature in the x- and y-axis. Table 45 shows CTE values for some commonly used PBGA materials.

Table 45. Examples of CTE of substrate and mold epoxy materials.

Material	Type of material	CTE in x- & y-axis [ppm / ºC]		Tg
		<Tg	>Tg	[ºC]
BT	Substrate	15	15	208
FR-4	PWB laminate	18	18	135
Material A	Mold compound	10	47	140
Material B	Mold compound	10	40	130
Material C	Mold compound	19	74	157
Material D	Mold compound	10	39	135

It is assumed that the materials parted are flexible enough with low internal stresses and that a segment of a sphere-form for the bi-material warpage can be expected. Fig. 47 shows a schematic presentation of a micro section of bi-material warpage. Now, the relationships presented below can be obtained from Fig. 47

$$\begin{cases} \frac{l_S}{2} = \frac{\mu}{360°} \times 2\pi \times r_S \\ \frac{l_{MC}}{2} = \frac{\mu}{360°} \times 2\pi \times r_{MC} \end{cases} \tag{38}$$

and

$$r_{MC} = r_S + t_{c-c}, \tag{39}$$

where l_S, l_{MC}, r_S, r_{MC}, $t_{c\text{-}c}$ and μ denotes the length of the substrate, the length of the mold compound, the radius of the substrate, the radius of the mold compound, the distance between the centres of the substrate and the mold compound and the angle of the curvature in degrees, respectively. It should be noted that the initial lengths of the substrate, $l_{0,S}$, and the mold compound should ($l_{0,MC}$) be the same.

The radius of curvature of the substrate r_S is needed to calculate the maximum warpage w. By using the right-angled triangle OA'B', Fig. 47, we can obtain

$$\begin{aligned} &\cos\mu = \frac{r_S - w}{r_S} \\ &\Leftrightarrow \\ &w = r_S - r_S \cos\mu = r_S(1-\cos\mu). \end{aligned} \tag{40}$$

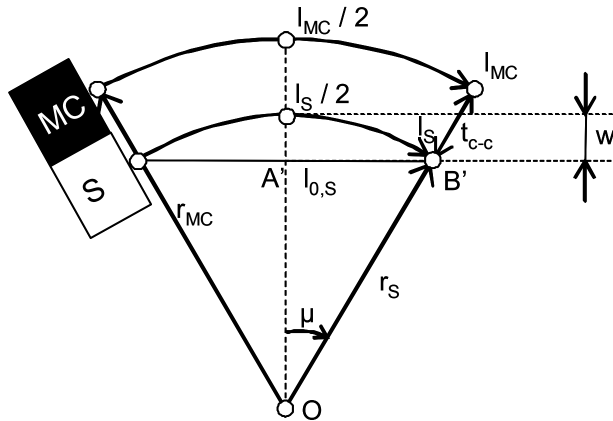

Fig. 47. A schematic presentation of a micro section of a bi-material warpage. The maximum warpage is denoted as *w*. The mold compound is denoted as *MC* and the substrate as *S*.

By entering the equations 37, 38 and 39 to Equation 40, we can finally obtain

$$w = \frac{l_{0,S}\left(1+\alpha_S \Delta T_S\right)\times t_{c-c}}{l_{0,MC}\left(1+\alpha_{MC}\Delta T_{MC}\right)-l_{0,S}\left(1+\alpha_S \Delta T_S\right)}\times \left(1-\cos\left(\frac{360^\circ}{4\pi}\times\frac{l_{0,MC}\left(1+\alpha_{MC}\Delta T_{MC}\right)-l_{0,S}\left(1+\alpha_S \Delta T_S\right)}{t_{c-c}}\right)\right). \tag{41}$$

The maximum warpage can thus be calculated by using only few parameters. The maximum warpages of the mold compound materials *"A"* to *"D"*, from Table 45, are presented in Table 46. The mold compound materials are jointed with Bismaleimide Triazine (BT) laminate with CTE of 15 ppm/°C. Results show that the higher glass transition temperature does not give lower warpage performance, as could first be assumed. The higher T_g mold compounds have higher CTEs above the T_g, which results to more warpage at elevated temperatures. Of the mold compound materials *"A"* to *"D"* the most promising would be the *"B"* and *"D"*, which have a relative low glass transition temperature, but their benefit is the lower CTE above the T_g.

Table 46. Maximum warpages of a BT substrate with four different mold compound materials at 260 °C with 25 × 25 mm substrate and mold compound area.

Variable		Mold compound			
		"A"	"B"	"C"	"D"
Tg [°C]		140	130	157	135
CTE [ppm/°C]	α_1	10	10	19	10
CTE [ppm/°C]	α_2	47	40	74	39
Warpage [µm]	Max	320	267	647	240
(+ convex, -concave)	Min	–56	–51	0	–54

To test the aforementioned method a warpage of the 27 × 27 mm^2 PBGA-component with "material *C*" from the Table 45 was predicted and measured. For the measurement a thermal shadow moiré method was utilized (*e.g.* Wang & Hassell 1997). 12 pieces of PBGAs were measured. The size of the die was 1.5% of the substrate area. The estimated and the measured maximum warpage in Fig. 48 show that the component packages already have approximately 100 micron concave warpage at room temperature. The predicted warpage is set to start from zero warpage. If this 100 micron concave warpage at the starting point is taken into consideration and the estimated values are shifted to correspond to the starting point of the measured values, one can conclude that the estimated values

cohere with the measured values. Also, the results show that the orientation of the warpage of the estimated and measured values coheres, when the 100 micron warpage offset is taken into account.

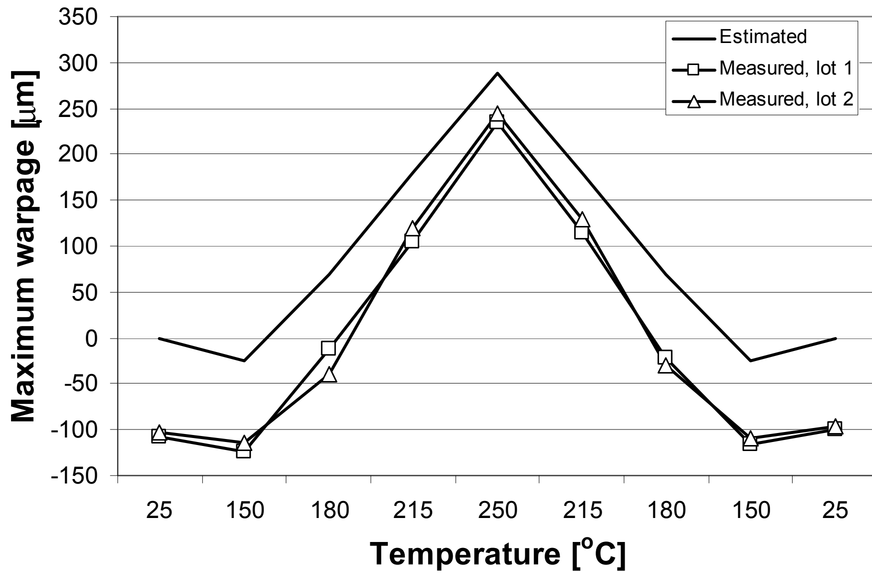

Fig. 48. The estimated and measured maximum warpage of a PBGA package during the lead-free reflow. The *lot 1* and *lot 2* included 6 samples; average warpage is shown for each temperature.

The maximum warpage of the component is dependent on the thermal properties of the *mold compound* and the *substrate*. The reflow peak temperature is higher in the lead-free reflow than in the conventional SnPb reflow. The actual difference seen by individual components depends on the multiple parameters, *e.g.* thermal mass of the board and components, the method for heat transfer and so on. The liquidus temperature is 34 °C higher in the lead-free (SnAgCu) reflow than in the conventional SbPb reflow process. In this Section, the peak temperatures of 220 °C and 260 °C for the SnPb and lead-free reflows were used, respectively (J-STD-020D 2007). So, for the same component the maximum warpage in the lead-free reflow should be higher than in the conventional SnPb-reflow process. To investigate the difference between these two reflow processes, Equation 41 was utilized in the estimation of the warpage of a 25 × 25 mm^2 PBGA with BT-substrate and mold compound material "*A*", Table 45.

The maximum warpage in the SnPb process is 182 μm, whereas in the lead-free it is 308 μm, Fig. 49. At the time of solidification, the warpage is 66 μm in SnPb reflow and 173 μm in lead-free reflow. This is a remarkable difference. For instance when using the 150 μm stencil thickness in the SMT process the estimated solder height falls roughly between 75 μm to 100 μm due to the flux evaporation. The warpage in the SnPb reflow is far below the solder height whereas it is even above the solder paste thickness in the lead-free reflow. The time above 100 μm warpage is two times longer in the lead-free reflow (60–120 seconds).

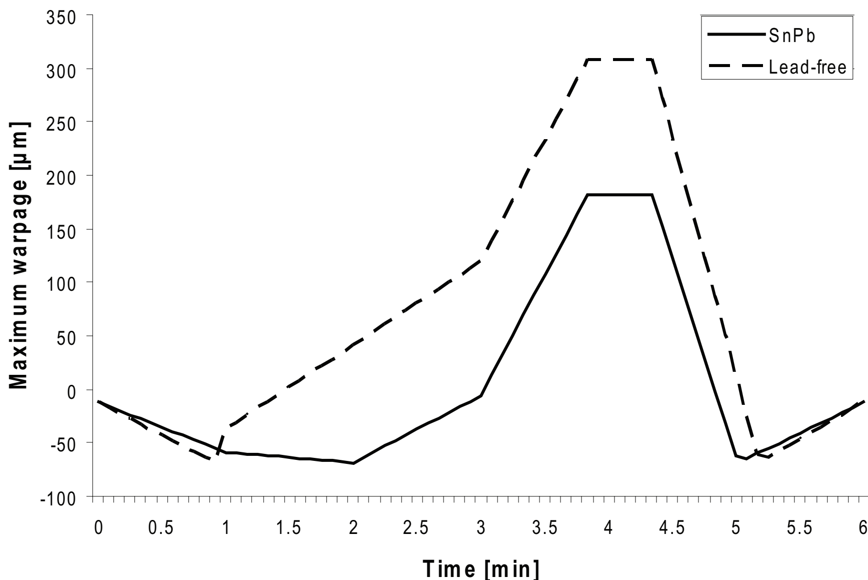

Fig. 49. The maximum warpage of a PBGA component in the SnPb and the Lead-free reflows, with peak temperatures of 220 °C and 260 °C, respectively. The rapid change in the warpage orientation at the 0.8 minutes is due to crossing the glass transition temperature and at the 1.0 minutes for the end of the preheat reflow zone.

To estimate the risk for soldering defects due to excessive warpage, the warpage level of at least equal to stencil thickness (150 μm) could be used as a lower limit for *constant defects*, Fig. 50. Below this component population might experience *random defects* due to the process and material quality and dimension variation.

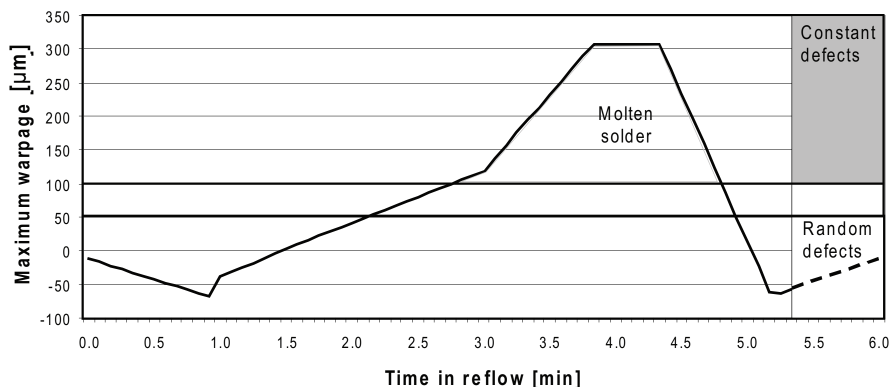

Fig. 50. A component warpage versus the time in lead-free reflow (peak temperature of 260 °C) estimated to the middle of the component.

In spite of the described limitations of the estimation method, the study showed that the proposed estimation method can be used for fast estimations of the risk levels of warpage defects. Also, the estimation method is especially useful for comparing the different reflow process temperatures setups and estimating the effect of new materials for component packages. Moreover, the measurements made for the PBGA component cohere well with the model predictions.

A segment of a sphere-form for the component warpage was as an assumption in the formula of the maximum warpage, which gave relatively accurate predictions, as was shown. The real cross sectional curvature for the component warpage would not be a perfect segment of a sphere, due to the stiff die in the middle of the component. By measuring the shape of the curvatures with different die sizes, the curvature fitting could be made and it could simply be a replacement for the curvature in Equation 38. This would give a better accuracy, but the circular (or spherical in three dimensions) curvature fitting could still give the same result during the reflow temperatures. These include the orientation of the warpage and the magnitude of the warpage in respect of the solder joint height. The accurate value of the maximum warpage is a secondary subject.

6.6 Conclusions

The effect of the interconnection and component materials and the solder paste volume variation on the characteristic life of the component interconnections were introduced and characterized. Also, a novel defect mechanism of the solder joints of the PBGA component was revealed. The solder joint defect is caused by material incompatibility of the PBGA component during the lead-free reflow. Moreover, a novel method for assessing the range of component warpage in the given process conditions was introduced.

The solder land geometry has an effect on the interconnection reliability. The level and the orientation of the effect are dependable on the shape of the solder joint. The measured and modelled effects of the characteristic life of the particular components were up to 30–44%, even with minor changes to the solder land geometries. Moreover, the +92% increase in characteristic life of leadless component was achieved with doubling (+83%) the solder land area. To conclude, the effect of the solder land geometries as a part of the reliability expectation of the whole product population can be high. This aspect might quite often be neglected, particularly when the component test board performance is transferred to reflect the real products that might have different solder land geometries in it. The solder paste volume variation study showed that the BGA components have a minor sensitivity to the applied solder paste volume variation. This is due to the fact that only 10% to 40% of the final solder is initiated from the solder paste. The CLLCC components are more sensitive for solder paste variation, as all of the solder is applied from the solder paste.

The bi-material warpage study showed that the estimation method can be used for fast estimations of the risk levels for warpage defects. Also, the estimation method is very useful for comparing the different reflow process temperatures setups and estimating the effect of the new materials for component packages. Moreover, the measurements made for the PBGA component cohere with the model predictions. The elevated soldering temperatures emphasize the warpage effect of PBGA components.

From the aforementioned qualities, the smallest impact to the solder joint lifetime is with the solder paste volume variation. Based on the results, the impact is below 10%. The next largest impact is based on the solder land geometrical design, where solder joint lifetime ratios are up to 90%. The effect of the solder material to the solder joint lifetime expectancy has the next greatest impact, up to +140%. The most important factor with respect to the solder joint reliability is the

level of stress generated into them. The effect of the warpage can not be characterized with respect to solder joint lifetime, due to the lack of its occurrence distribution model.

Altogether, the BGA and the CLLCC components response to the type of solder joint material, to the solder paste volume variation, to the solder land geometry dimensions and to the stress level diverges with respect to the solder joint reliability.

7 Summary of thesis

In this thesis, a method to predict the second level interconnection failure occurrence is introduced. The method utilizes the second level reliability test data to the hazard rate predictions of the component solder joints. The results of the method can be used as a part of product field performance estimates. Also, the effect of the process variation and the material properties on lead-free solder joint reliability is introduced

The effect of the parameters of an interconnection system is often neglected, when the stress test performance is interpreted to the real usage environments. These parameters include at least the material properties of the PWB, the solder and the component together with the geometrical dimensions of the solder and the product stress conditions. It can also be highlighted that the accelerated stress test is only a part of a comprehensive interconnection reliability analysis. Without taking the aforementioned parameters into consideration, a true reliability assessment of the component interconnections can not be made. For instance, the effect of a single parameter on the characteristic life of component interconnection is estimated to be up to +140%, or even more. So, the accelerated stress test is a sub-phase of comprehensive reliability analysis.

While the conventional interconnection reliability analyses are somewhat inaccurate, the methods presented in this thesis enable a true comparison of the component packaging technologies to each other. This benefit will be emphasized with the component technologies, which are not suitable for a wide range of usage conditions. Also, without knowing the stress levels experienced by the component interconnections, the reliability can not be given exactly. This makes the interconnection reliability analysis complex as was stated in the *Chapter 3.*

A novel method of estimating the interconnection failures in terms of costs is presented in *Chapter 4*. The reliability and cost analysis show that a comprehensive analysis is needed to fully understand the risks involved in the different packaging technologies. The analyses also show that the stress environment must accurately be known, or the costs of the interconnection failures could be tremendous. This analysis method is strongly recommended to be further developed, as it has a great potential in the product development. More emphasis could be put in finding the corresponding cost model for the interconnections.

A novel method of interpreting the qualification test data into failure occurrence estimates is presented in *Chapter 5*. The idea is to use a component

packaging type specific approach instead a conventional generic approach. Moreover, the intent is to use readily calculated multipliers in order to estimate the hazard rate of the component interconnections in the given operational conditions. This is made possible by estimating the stress conditions in the test vehicle and in the actual product. Furthermore, novel qualification criteria were introduced in *Chapter 5*. Instead of using the generic qualification criterion for all of the different component packaging types, the component packaging specific criteria should be used. These criteria are intended to describe the true failure behaviour of the component interconnections in the actual operational conditions. The benefit of such a method is to be able to estimate the usage of particular component in the given stress conditions and avoid over-specification or over-designing. The future work should concentrate on finding constitutive models for different component packages and on verifying the solder joint hazard rates in different usage conditions.

A novel defect mechanism of the solder joints of a PBGA component is also revealed. The defects are caused by an excessive warpage of component during the lead-free reflow. The warpage study shows that the presented novel method can be used for accurate estimations of the maximum warpage, *Chapter 6*. These defects can be avoided with proper material and process parameter design. Furthermore, the estimation method is very useful in comparing the different reflow process temperature profiles and in estimating the effect of the new materials for component packages. Moreover, the measurements made for the PBGA component cohere with the model predictions. It is also shown that the elevated soldering temperatures emphasize the warpage effect of the PBGA components. Even the model gives relatively accurate warpage predictions; more development is needed to take the effect of the larger dies into consideration or more complex component structures.

In this thesis a novel method to utilize the accelerated stress test data for the hazard rate estimates is introduced. The hazard rate expectations of the interconnection elements are presented as interconnection failures in time (i-FIT) figures that can be used as a part of the conventional product reliability estimates. The method utilizes a second level reliability test results for a packaging type specific failure occurrence estimates. The benefit of such a method compared to the earlier published methods is the ability to use the stress test data for the end usage hazard rate estimates. Furthermore, the results can be used as such in the component packaging reliability estimates.

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Appendix 1 Component material parameters used in this thesis

Table 47. The material properties and dimensions for leaded components in the Chapter 4.

Material property		TSOP_A42	TSOP_Cu
Unideality factor (leaded)	F_u	1	1
Component thermal expansion coefficient	$\alpha_{Component}$ [ppm/°C]	12	12
PWB thermal expansion coefficient	α_{PWB} [ppm/°C]	18	18
Width of the solder wetted area	W [mm]	0.28	0.28
Length of the solder wetted area	L [mm]	0.4	0.4
Diagonal flexural strength	K_d	2	1
Solder paste stencil thickness	2h [μm]	150	150
Maximum distance between two pins	$2L_D$ [mm]	21.1	21.1
Fatigue ductility coefficient	$2\varepsilon'f$	0.558 *	0.558 *

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Table 48. The material properties and dimensions for leadless components in the Chapter 4.

Parameter *	Component				
	BGA1	BGA2	BGA3	CLLCC_D	CLLCC_Q
F	1	1	1	0.7	0.7
α_{Comp}	15	14	15	6.5	6.5
α_{PWB}	18	18	18	18	18
h	0.45	0.35	0.45	0.15	0.15
$2L_D$	36.8	26.9	31.1	7.1	10.3
A_s	0.149	0.149	0.149	0.0884	0.0884
B_s	–0.0794	–0.0794	–0.0794	0.13	0.13

	μbga	LLP	0201	0402	0603
F	1	1	1	1	1
α_{Comp}	13.5	17	6.5	6.5	6.5
α_{PWB}	18	18	18	18	18
h	0.25	0.075	0.04	0.06	0.075
$2L_D$	22.6	17	0.6	1	1.6
A_s	0.149	0.179	0.0884	0.0884	0.0884
B_s	–0.0794	–0.0953	0.13	0.13	0.13

Table 49. The parameters of a BGA component in Chapter 5.

Parameter *	η (cycles)					
	400	500	700	1000	2000	5000
F_u	1	1	1	1	1	1
α_{Comp}	11.75	12.3	12.3	13.1	13.2	14.3
α_{PWB}	18	18	18	18	18	18
h	0.35	0.35	0.4	0.4	0.4	0.45
$2L_D$	36.8	36.8	36.8	36.8	28.3	28.3
A_s	0.179	0.179	0.179	0.179	0.179	0.179
B_s	–0.0953	–0.0953	–0.0953	–0.0953	–0.0953	–0.0953

Table 50. The parameters of a CLLCC component in Chapter 5.

Parameter *	η (cycles)					
	400	500	700	1000	2000	5000
F	1	1	1	1	1	1
α_{Comp}	8	8	9	9	10	12
α_{PWB}	18	18	18	18	18	18
h	0.25	0.25	0.25	0.25	0.25	0.25
$2L_D$	11.7	10.7	10.3	8.9	7.5	6.9
A_s	0.0884	0.0884	0.0884	0.0884	0.0884	0.0884
B_s	0.13	0.13	0.13	0.13	0.13	0.13

Table 51. The parameters of a bottom termination plastic substrate component in Chapter 5.

Parameter *	η (cycles)					
	400	500	700	1000	2000	5000
F_u	1	1	1	1	1	1
α_{Comp}	13.3	13.7	14.25	14	14	15.25
α_{PWB}	18	18	18	18	18	18
h	0.1	0.1	0.1	0.1	0.1	0.1
$2L_D$	14	14	14	11.3	8.5	8.5
A_s	0.179	0.179	0.179	0.179	0.179	0.179
B_s	–0.0953	–0.0953	–0.0953	–0.0953	–0.0953	–0.0953

Table 52. The parameters of a Ceramic BGA component in Chapter 5.

Parameter *	η (cycles)					
	400	500	700	1000	2000	5000
F_u	1	1	1	1	1	1
α_{Comp}	7	7	7	7	7	7
α_{PWB}	18	18	18	18	18	18
h	0.8	0.8	0.8	0.8	0.8	0.8
$2L_D$	34	31	27	23.3	17.5	12
A_s	0.0884	0.0884	0.0884	0.0884	0.0884	0.0884
B_s	0.13	0.13	0.13	0.13	0.13	0.13

Table 53. The parameters of a Cu-leaded TSOP component in Chapter 5.

Parameter *	η (cycles)					
	400	500	700	1000	2000	5000
F_u	1	1	1	1	1	1
$\alpha_{Component}$	10.99	10.8	11.11	11.39	11.98	12.99
α_{PWB}	18	18	18	18	18	18
W	0.28	0.28	0.28	0.28	0.28	0.28
L	0.4	0.4	0.4	0.4	0.4	0.4
K_d	2	2	2	2	2	2
2h	150	150	150	150	150	150
$2L_D$	21.5	20	19.5	18.9	18	17.9
A_s	0.0884	0.0884	0.0884	0.0884	0.0884	0.0884
B_s	0.13	0.13	0.13	0.13	0.13	0.13

Table 54. The parameters for method validation in Chapter 5. TC denotes to Thermal Cycles in the test.

Parameter [*]	Component			
	BGA1356	CBGA552	MLF48 [*]	CLLCC10
F	1	1	1	0.7
α_{Comp}	15	6	14	6.5
α_{PWB}	18	18	17	18
h	0.43	0.74	0.15	0.175
$2L_D$	50.9	28.3	9.9	9
A_s	0.299	0.1838	0.149	0.1838
B_s	–0.816	–0.277	–0.0794	–0.277
η_{test}	752 TC[**]	789 TC[**]	5090 TC[***]	801 TC[**]
number of samples	28	12	12	17
Solder	SnPb	SnPb	SnPb	SnPb

[*] Syed & Kang, 2003; [*] –40 °C to +125 °C, 24 cycles per day; [***] –55 °C to +125 °C, 48 cycles per day

Parameter		Explanation
F, F_u		Unideality factor
α_{Comp}	[ppm/°C]	Thermal expansion coefficient of component
α_{PWB}	[ppm/°C]	Thermal expansion coefficient of PWB
h	[mm]	Solder joint height
$2L_D$	[mm]	Maximum distance between two pads
A		Material constants for the stress dependent fatigue
B		ductility coefficient
W	[mm]	Width of the solder wetted area
L	[mm]	Length of the solder wetted area
K_d	[m/N]	Diagonal flexural strength
2h	[µm]	Solder paste stencil thickness
$2\varepsilon'f$		Fatigue ductility coefficient

Appendix 2 Environmental acceleration factors by MIL-HDBK-217F (1991)

Table 55. Environmental acceleration factors / MIL-HDBK-217F (1991).

Environment	Short Description	Environment factor
Ground, Benign	Non mobile, temperature and humidity controlled environment	1.0
Ground, Fixed	Moderately controlled environments	4.0
Ground, Mobile	Equipment installed on wheeled or tracked vehicles	25
Naval, Sheltered	Sheltered or below deck conditions	12
Naval, Unsheltered	Unprotected equipment exposed to weather conditions and immersed in salt water	35
Airborne, Inhabited, Cargo	Environment extremes of pressure, temperature, shock and vibration	28
Airborne, Inhabited, Fighter	Environment extremes of pressure, temperature, shock and vibration	42
Airborne, Uninhabited, Cargo	Severe environment extremes of pressure, temperature, shock and vibration	58
Airborne, Uninhabited, Fighter	High performance aircraft, environment extremes of pressure, temperature, shock and vibration	73
Airborne, rotary winged	Equipments on helicopters	60
Space, Flight	Earth orbital	1.1
Missile, Flight	Air breathing missiles	60

Appendix 3 Multipliers for different failure levels

The prediction of the failure level at the *x-%* can be derived from the Equation 10 as follows:

$$A.F.(x\%) = \frac{N_f\left(x\%\right)}{N_f\left(characteristic_life\right)} = \left(\frac{\ln\left(1-0.01x\right)}{\ln\left(\frac{1}{e}\right)}\right)^{1/\beta}, \qquad (42)$$

where $N_f(x\%)$ and $N_f(characteristic\ life)$ are the number of cycles to failure at the reference criterion and at the characteristic life, respectively. β denotes the Weibull shape parameter. Table 56 shows multipliers for different failure levels as a function of Weibull shape parameter.

Table 56. Multipliers for different failures levels (cdf) as a function of Weibull shape parameter β. η (63.2%) denotes the Weibull characteristic life.

cdf (%)	Multiplier / Weibull shape parameter			
	β = 2	β = 4	β = 8	β = 16
0.001	0.003	0.056	0.24	0.49
0.01	0.010	0.10	0.32	0.56
0.1	0.032	0.18	0.42	0.65
1	0.10	0.32	0.56	0.75
10	0.32	0.57	0.75	0.87
50	0.83	0.91	0.96	0.98
η (63.2)	1.00	1.00	1.00	1.00
90	1.52	1.23	1.11	1.05
95	1.73	1.32	1.15	1.07
99	2.15	1.46	1.21	1.10

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