

INTEGRATED RF BUILDING BLOCKS FOR BASE STATION APPLICATIONS

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FOR BASE STATION APPLICATIONS**

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Abstract

This thesis studies the level of performance achievable using today's standard IC processes in the integrated RF subcircuits of the modern GSM base station. The thesis concentrates on those circuit functions, i.e. I/Q modulators, variable gain amplifiers and frequency synthesizers, most relevant for integration in the base station environment as pinpointed by studying the receiver/transmitter architectures available today.

Several RF integrated circuits have been designed, fabricated and their level of performance measured. All main circuits were fabricated in a standard double-metal double-poly 1.2 and 0.8 μm BiCMOS process. Key circuit structures and their measured properties are: 90° phase shifter with 1° phase error with VCC = 4.5...5.5 V and T = -10...+85 °C, I/Q modulator suitable for operation at output frequencies from 100 MHz to 1 GHz and baseband frequencies from 60 to 500 kHz (2.0 mm 2.0 mm, 100 mA, 5.0 V) with LO suppression of 38 dBc and image rejection of 41 dBc, temperature compensated DC to 1.5 GHz variable gain amplifier (1.15 mm 2.00 mm, 100 mA, 5.0 V) with a linear 50 dB gain adjustment range, maximum gain of 18.5 dB and gain variation of 1 dB up to 700 MHz over the whole operating conditions range of VCC = 4.5...5.5 V and T = -10...+85 °C, a complete bipolar semicustom synthesizer (90...122 mA, 5.0 V) and two complete full-custom BiCMOS synthesizer chips including all building blocks of a PLL-based synthesizer except for the voltage controlled oscillator and the loop filter. The synthesizers include circuit structures such as ~2 GHz multi-modulus divider and low-noise programmable phase detector/charge pump (18.7 pA/ $\sqrt{\text{Hz}}$ at $I_{\text{out}} = 500 \mu\text{A}$) and have an exemplar phase noise performance of -110 dBc/Hz at 200 kHz offset.

One of the main problems of the integer-N PLL based synthesizer when used in a multichannel telecommunications system is the level of spurious signals at the output, when the synthesizer is optimised for fast frequency switching. Therefore, a method using only two current pulses to make the frequency step response of the loop faster, thus allowing a narrower loop bandwidth to be used for additional spur suppression, is proposed. The operation of the proposed speed-up method is analysed mathematically and verified by measurements of an existing RF-IC synthesizer operating at 800 MHz. Measurements show that simple current pulses can be used to speed up the channel switching of a practical RF synthesizer having a frequency step time in the tens of μs range. In the example, a 7.65 MHz frequency step was made seven times faster using the proposed method.

Keywords: frequency synthesizers, modulators, RF circuits, transceiver architectures, variable gain amplifiers

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I wish to express my gratitude to Professor Juha Kostamovaara, who has supervised this work and led the research projects in which it was done, for his tireless encouragement, guidance and example.

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Oulu, December 2002

Juha Häkkinen

List of original papers

- I Häkkinen J, Rahkonen T & Kostamovaara J (1996) A 925-960 MHz I/Q modulator in a 8 GHz 1.2 μm BiCMOS process. *Journal of Analog Integrated Circuits and Signal Processing* 9(1):39-53.
- II Häkkinen J, Rahkonen T & Kostamovaara J (1995) A 100 MHz to 1 GHz Variable Gain Amplifier in A 8 GHz 1.2 μm BiCMOS Process. *Proceedings of the 13th Norchip Seminar, November 7-8 1995, Copenhagen, Denmark*, 1:169-176.
- III Häkkinen J, Rahkonen T & Kostamovaara J (1996) A Temperature Compensated 100 MHz to 1 GHz Variable Gain Amplifier in a 8 GHz 1.2 μm BiCMOS Process. *Proceedings of IEEE International Symposium on Circuits and Systems, May 12-15 1996, Atlanta, USA*, 1: 183-186.
- IV Häkkinen J, Rahkonen T & Kostamovaara J (1996) An Integrated 100 MHz to 1 GHz I/Q Modulator with CML Phase Shifter. *Proceedings of the 1st IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design, September 13-14 1996, Pavia, Italy*, 1:11-15.
- V Häkkinen J, Rahkonen T & Kostamovaara J (1998) Comparison of two integrated BiCMOS 950 MHz direct I/Q modulators. *Journal of Analog Integrated Circuits and Signal Processing*, 15(1):71-83.
- VI Häkkinen J, Rahkonen T & Kostamovaara J (1998) A 100 MHz to 1 GHz Variable Gain Amplifier in a 8 GHz 1.2 μm BiCMOS Process. *Journal of Analog Integrated Circuits and Signal Processing*, 15(2):169-181.
- VII Häkkinen J, Rahkonen T & Kostamovaara J (1998) A Bipolar Semicustom PLL Based Synthesizer for GSM and DCS Systems. *Proceedings of the IEEE International Symposium on Circuits and Systems, May 31 - June 3 1998, Monterey, California, USA*, 4:413-416.

- VIII Häkkinen J, Rahkonen T & Kostamovaara J (1999) A Frequency Hopping Synthesizer Chip for GSM and DCS Systems. Proceedings of the 41st Midwest Symposium on Circuits and Systems, August 9-12 1998, South Bend/Notre Dame, Indiana, USA, 356-359.
- IX Häkkinen J, Rahkonen T & Kostamovaara J (1999) A Frequency Hopping Synthesizer IC for IF and RF Applications. Proceedings of the IEEE International Symposium on Circuits and Systems, May 30 - June 2 1999, Orlando, Florida, USA, 1:202-205.
- X Häkkinen J, Rahkonen T & Kostamovaara J (1999) An Integrated Low-Noise Programmable Charge Pump. Proceedings of the 6th International Conference on Electronics, Circuits and Systems (ICECS '99), September 5 - 8, 1999, Pafos, Cyprus, Greece, 185-188.
- XI Hakkinen J & Kostamovaara J (2001) Speeding Up the PLL Frequency Step Response by Two Charge Pulses. *Electronic Letters* 37(7): 411-412.
- XII Hakkinen J & Kostamovaara J (2001) Speeding up an Integer-N PLL by Controlling the Loop Filter Charge. Accepted (with revisions) for publication in the *IEEE Transactions on Circuits and Systems, II Analog and Digital Signal Processing*.

The research work described in these papers was carried out at the Electronics Laboratory, Department of Electrical Engineering and Infotech Oulu, University of Oulu, Finland. The work was done mainly in the research projects RF-ASIC 1993-1994, RF-ASIC II 1994-1995, ERFMI 1995-1996, FAMIC 1996-1997, NOPSA 1997-1998 and TIMIC 1998-2000, which were funded by the University of Oulu, TEKES and several industrial companies. These projects were headed by Prof. Juha Kostamovaara who also supervised this work.

The research reported in the original papers was carried out by the author, who also prepared the manuscripts.

Papers I and IV describe the developed I/Q modulator circuits for direct up-conversion applications in a GSM base station and paper V compares the performance of these modulators to each other and some other similar designs reported in the literature.

Papers II, III and VI report the development of the variable gain amplifier circuits for base station transmitter architectures, during which two separate ICs were designed and results published individually in the papers.

The development of the synthesizer circuits for RF and IF frequency synthesis applications in the base station is reported in papers VI through X. This research includes a general purpose BiCMOS synthesizer reported in paper VII, a bipolar semicustom synthesizer chip described in paper VIII, and a more specialized and optimized BiCMOS synthesizer described in paper IX. The design of the low-noise high output resistance charge pump developed for the synthesizer reported in paper IX is described separately in paper X.

A new way to make the frequency step response of a PLL based synthesizer faster using simple current pulses is proposed in paper XI. A more thorough account of the development, mathematical treatment and experimental verification of the proposed method is given in paper XII.

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1 Introduction

1.1 Background

The rise of the wireless telecommunications industry has created a growing need for integrated RF electronics. However, the level of integration of the RF circuitry of telecommunications systems has so far been low compared to the level of integration of the IF and especially the baseband parts of such systems. Especially the lack of high-quality inductors has limited the overall level of integrability of RF functions within conventional RF receiver architectures such as the well-known superheterodyne. The need for further integration has led to the invention of modified and new RF architectures. However, regardless of the architecture one can find a set of basic RF subcircuits or circuit functions, such as mixers, I/Q mixers, filters, low-noise amplifiers, frequency synthesizers and power amplifiers that can be found in almost any receiver/transmitter architecture.

Integrated circuits, like other electronic circuits, can roughly be divided into two categories depending on the operating frequency, namely low and high frequency circuits. Their division is somewhat ambiguous, since the limit of high frequency operation is not well defined. However, the circuits operating at the high end of the frequency spectrum are traditionally called radio frequency circuits or RF-circuits, because they perform functions often associated with high frequency radio telecommunications or radar systems. A more formal definition of RF circuits is given as the ratio of the physical dimensions of the circuit (e.g. chip or PCB) and the wavelength of the information carrying a signal in the respective medium (e.g. GaAs in some monolithic microwave integrated circuits or fibreglass in everyday PCBs):

$$\frac{d_{\max}}{\lambda_s} < \frac{1}{10} \quad \text{or} \quad f_s < \frac{1}{10} \frac{v_s}{d_{\max}}, \quad \text{where} \quad (1)$$

d_{\max} = maximum electrical dimension within the circuit, f_s = signal frequency, λ_s = corresponding wavelength and v_s = speed of the signal in the respective medium. Thus, equation (1) gives a rough limit frequency f_s , above which the RF theory must be employed during circuit design.

However, for the purpose of this thesis a somewhat different definition is used, because due to the small dimensions of the circuit (e.g. $d_{max} \sim 3$ mm) equation (1) indicates that the use of RF design methodology is not necessary inside an integrated circuit at frequencies around a few GHz ($\lambda_s \sim 150$ mm). Thus, in the following chapters the term RF-circuit means those analogue circuit structures commonly encountered in modern radio telecommunication circuitry performing operations on the information carrying signal outside the intermediate frequency (IF) stages and baseband signal processing. However, in the near future many of the traditional IF structures, for example, may enter the RF domain, as their speed of operation increases. This could be true with high-speed ADC converters and dividers, for example.

The main motivation behind RF integration is similar to the integration of any type of circuitry. The benefits of integration include smaller size, lower cost, smaller power consumption and enhanced reliability. The integration of RF functions makes the overall design of the system simpler, because the interstage matching needed to minimize signal reflections can often be omitted inside an integrated circuit contrary to discrete design (noise matching may still be required, for example). However, most standard IC processes lack high-quality integrated inductors usable for matching, LC resonators and filtering, the shortcoming of which also has often been the limiting factor in the level of integration. This poses a great challenge for the future RF integration as the overall systems, possibly hand-held, to get smaller and the production volumes larger with increased reliability requirements.

1.2 Aim and contents of the work

Due to different specifications and operating environment, the level of integration has traditionally been much lower in the base station end of a modern radio telecommunications system than in the mobile units. However, the integration of the RF functions of the base station becomes more attractive as cell sizes shrink and power levels drop (e.g. micro cells and office level applications). This thesis deals with the integration of the RF circuitry from the base station point of view.

To achieve optimum performance, it makes no sense today in the base station environment to integrate the whole transceiver circuitry into one chip. Therefore, this thesis concentrates more on the integrated realization of the fundamental building blocks of different RF architectures rather than on the complete integration of the transceiver circuitry. The common RF building blocks of transceiver architectures are identified in the beginning of Chapter 2 by reviewing different transmitter and receiver architectures currently available. Different ways to realize some of these building blocks in an integrated form are reviewed in more detail in the end of Chapter 2.

Chapter 3 gives a brief review of the actual RF-IC design process.

Chapter 4 gives an overview of the various circuit structures – I/Q modulators, variable gain RF amplifiers and synthesizers – and their performance reported in the original papers. The specifications of these blocks are based on existing GSM base station transceiver building blocks, and the aim of the work is to provide the same level of

performance with custom-made integrated solutions that is now achieved with mixed discrete and integrated circuitry.

One of the basic problems of the well-known integer-N type PLL synthesizer, namely the trade-off between the lock-in time and the level of reference spurs in the output spectrum, is discussed in more detail in Chapter 5. Especially in multichannel systems the level of reference spurs must be made low, so that they do not disturb the adjacent channels. The level of the spurious signals can be made lower by reducing the loop gain at the respective frequency by reducing the loop bandwidth, for example. However, this makes the loop slower, which may not be acceptable in frequency hopping applications (e.g. systems utilizing time-domain duplexing). In Chapter 5, both a theoretical look and experimental results of a collection of methods based on the control of the loop filter charge are presented which aim to alleviate this speed vs. spurious signal problem. This will lead to the introduction of a new speed-up method using simple current pulses superimposed on the loop filter as described in more detail in papers XI and XII.

2 Transmitter and receiver architectures in a modern radio communications system

2.1 Overview

All modern radio telecommunication systems operate within an environment bound by physical laws, system properties and man-made regulations. Physical rules, such as the way in which the radio waves propagate through the medium between the transmitter and the receiver or the noise generated in a resistor, set the fundamental limits, under which all telecommunication systems and their various building blocks must operate. The capacity of the system, that is the number of channels allocated for a given geographical area, for example, is a system property, which directly affects the way in which the individual parts of the system may be constructed. Because the frequency spectrum suitable for radio telecommunications is in itself a limited resource, national and international regulations allocate only a narrow bandwidth for each telecommunications system. Thus, most modern telecommunications systems share some common denominators, such as multiple carriers closely spaced within a relatively small overall system bandwidth with possible interferers from natural sources or from other radio systems and the large dynamic range of signals due to the properties of the multi-path

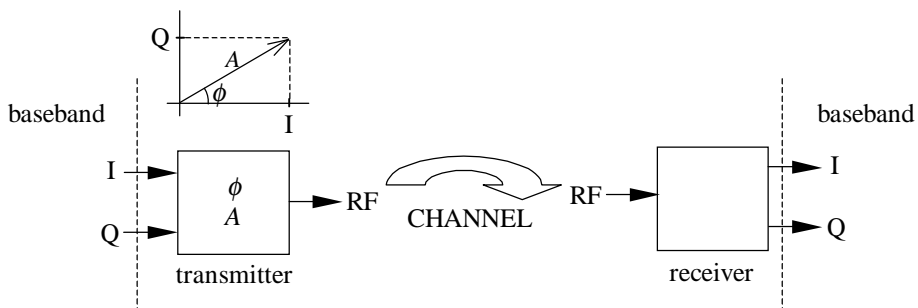


Fig. 1. Generic receiver and transmitter in a radio telecommunications system.

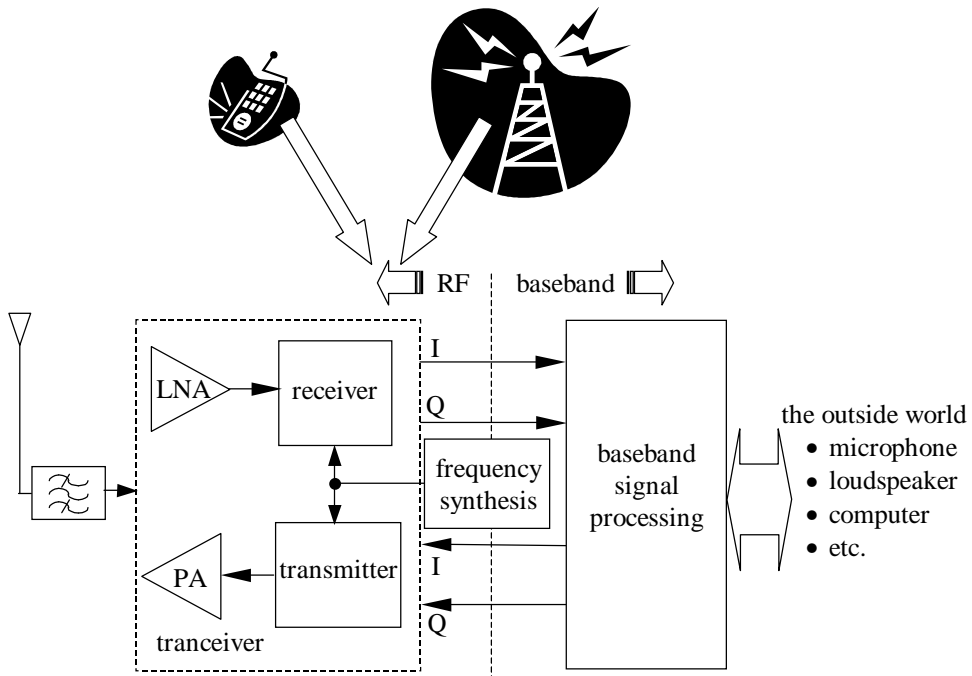


Fig. 2. Structure of a generic telecommunication unit.

fading channel and varying distance between the transmitter and the receiver.

The above factors have led to the use of complex modulation methods, which are best suited for narrowband, multiple channel systems. The generic transmitter and the receiver, and their location in a radio telecommunication system, can be represented schematically as in Fig. 1. In the generic transmitter, the phase and possibly the amplitude of the RF signal are controlled by the so-called in-phase and quadrature, or more shortly I and Q signals, the properties of which determine the type of modulation. The actual data symbols to be transmitted are coded to the I and Q signals in baseband circuitry. In the generic receiver the transmitted symbols are decoded by recovering the original I and Q signals from the received RF signal. In practice, the various architectures used to realize the functionality of the transmitter and receiver must address not only the problems associated in the theoretical generation of the desired modulation/demodulation, but also usually more demanding evils related to the properties of the channel and to the non-idealities of the building blocks. Additionally, the practical realizations of the transmitter and the receiver within the otherwise similar overall structures of the mobile unit and the base station shown in Fig. 2., diverge due to the different driving forces behind their development.

The integration of the transmitter and receiver of the mobile unit is extremely desirable, because such things as extended battery life, reduced weight and size which make the hand-held unit more desirable for the customer, are easily accommodated by increased level of integration. Prize and reliability of the complete unit are also directly influenced by the integration of multiple functions into a single chip and the mass production of ICs. The need to include more RF functionality within the same space

inside a hand-held unit, as in the case of a dual-band unit, for example, may make further integration unavoidable. The ultimate goal is the integration of the complete RF front-end into a single, preferably CMOS, transceiver chip with no external components and capability to operate in all systems without modifications. This concept is best realized, if the digitization of the RF signal can be performed as close to the antenna as possible and the different systems facilitated in DSP/software, i.e. the so called software radio.

In contrast, the integration of all RF functions of the base station into a single chip is not as desirable – due to the less strict restrictions in size or power consumption, the same driving forces as with the hand-held unit are not there. Besides, since a single base station serves a large number of customers at any given time, the integration cannot be made at the cost of performance or reliability (e.g. the synthesizer noise and lock-in time specifications of the GSM base station may be a couple of decades tighter than those of the hand-held unit). Contrary to the hand-held unit, it may not be desirable to use the same IC technology for all RF structures either, because this can compromise the performance of some parts of the system. Thus, for example, the choice of low-noise/high-linearity yet expensive GaAs or SiGe technology, either in an integrated or discrete form, for the LNA and the PA circuitry can be justified. If the rest of the RF circuitry is integrated using BiCMOS or CMOS, this will directly lead to a system where the given RF architecture is realized with multiple ICs. Having said that, there are, however, several reasons, why even the front-end of a base station will benefit from increased level of integration. Reliability and prize are two of these issues. Even size reduction may be sought as cell sizes get smaller and base stations find their home even indoors as in some office-scale applications. In these cases the requirements of the RF front-end of the base station and the hand-held unit will become increasingly similar.

Even when the integration of RF structures is deemed necessary and worthwhile, it might be hard to transform existing receiver and transmitter architectures directly to an integrated form. For example, the most dominant pre-integration era RF receiver topology, namely the super heterodyne architecture, is not very well suited for integration, because it requires numerous high-quality filters not easily realizable in an integrated form. The poor quality of integrated components also compromises the performance of individual transceiver building blocks, such as oscillators and VCOs. Even if the superheterodyne receiver could be integrated with adequate performance, the architecture is quite complex and thus may not be the optimum one as matters such as size and power consumption are of great importance. Thus, the direct integration of existing RF architectures does not automatically produce optimal solutions, which has turned the designers' attention to alternative and new architectures. These architectures are studied in more detail in sections 2.2 and 2.3.

The new receiver architectures presented in chapter 2.2 find their home mainly in hand-held units, where the increase in the level of integration is most desirable. However, since the performance of the base station receiver cannot be compromised and the size and power consumption are not main issues, the superheterodyne architecture remains in many cases the preferred receiver topology. High Q value SAW filters can readily be used and the core transceiver chip surrounded with LNA and PA circuitry with optimum selection of technologies and discrete/integrated solutions. Contrary to this, the selection of the transmitter architecture (see chapter 2.3) in both the hand-held unit and the base stations is not as straightforward, since no single architecture is superior to another when size, power consumption, isolation etc. are compared.

What factors then limit the integration of existing and new RF architectures? The most often encountered technological problem is the lack of high-quality inductors and transformers most useful for the kind of low-noise/low-voltage narrowband systems we are discussing here. This problem may disappear in the future as technologies with highly resistive substrate materials, such as GaAs and SOI, bring high Q values to reality. However, the usability of such exotic processes might be damaged especially in consumer products by their high fabrication costs. New architectural and circuit level innovations may enable the fabrication of high-performance circuits with existing low Q value components.

A single technology, such as CMOS for example, may not be the optimum choice for every building block of the given architecture. Thus, for optimum performance the LAN and the PA might be made using GaAs technologies rather than CMOS used for the rest of the transceiver circuitry. This will directly lead to a system where the given RF architecture is realized with multiple ICs.

When integrated into a single chip, the various building blocks and the complete architecture must cope with the completely new operating environment that it faces inside the silicon chip. Factors, such as parasitic capacitances, resistances and inductances, noise coupled via the semi-conducting substrate and power supply lines, all of which are hard to model in manual calculations and simulations, may degrade the performance of the transceiver beyond usability. The situation becomes even more complicated if the transceiver structures coexist in the silicon with digital circuitry, as in mixed-mode ICs. Due to common mode noise, the receiver structures may have to be made differential, which increases power consumption and size. Accurate dimensioning of integrated structures is hard, because absolute values of integrated components can vary tens of percents and since trimming of integrated components is almost out of the question in mass production. All this makes the development of RF-ICs time-consuming and expensive.

The lack of properly trained engineers might also be a problem. Most of the experienced RF engineers date to the days, when the transceiver parts were made of discrete components and the obvious receiver architecture was the superheterodyne receiver. On the other hand, the traditional analog IC designer has little or no RF knowledge at all, but is familiar with the problems associated to the IC environment. Thus, the designer of RF transceivers needs the understanding of both of these fields, familiarity with the various, possibly new, transmitter/receiver architectures and maybe even some familiarity with digital techniques, as in the case of frequency synthesizer design, for example. The understanding of DSP would also make the dialogue between the RF designer and the baseband designer more fruitful, which might lead to new, system-wide optimized architectures.

2.2 Receiver topologies

The receiver of a modern radio telecommunications system has to tackle with many difficulties rising either from the environment where the receiver has to operate or from the fundamental properties of various circuit functions and the non-idealities of their real

life implementations. Complexity, cost, power dissipation and the number of components are some of the criteria used to evaluate the pros and cons of various architectures.

The basic function of any receiver is to distinguish the desired signal from all other signals and to amplify the signal to a sufficient level for reliable detection. The simplest form of such a receiver would be a bandpass filter tuned to the same frequency with the signal. Note that this filter should in practice be a tunable one or there would have to be a bank of bandpass filters with different centre frequencies, if any kind of channel selection was desired. However, this would indeed be a possible solution to the problem, if the desired signal were occupying part of the frequency spectrum devoid of any other interfering signal. Unfortunately, this is not the case in modern telecommunications systems, where a fairly narrow frequency band is allocated for many closely spaced channels. Thus, as shown in Fig. 3., the desired signal, which may be very weak due to distance and/or a fading channel, may be surrounded by other, possibly as much as ~ 100 dB stronger, signals from neighbouring channels that cannot be sufficiently attenuated. The detection of a weak desired signal in the presence of strong interferers requires a large dynamic range from the receiver. Furthermore, since the bandwidth allocated for one channel is extremely narrow compared to the frequency of the carrier, the quality factor of the channel select filter would have to be extremely high. Because it is very hard or downright impossible to manufacture, at least in an integrated form, bandpass filters with a high enough quality factor, designers of radio receivers have been trying to circumvent the channel selection problem by clever architectural innovations, some of which will be described in the following paragraphs.

2.2.1 Heterodyne architecture

The operating principle of the well-known heterodyne receiver developed by Armstrong is shown in Fig. 4. (Armstrong 1920). In this receiver architecture the need of an extremely narrow-band channel select filter centred around the carrier frequency (ω_1) is circumvented by performing the channel selection at a lower frequency (ω_2). Because the bandwidth of the channel select filter, now operating at a lower frequency, remains unchanged, the quality factor decreases, which makes the manufacturing of the filter

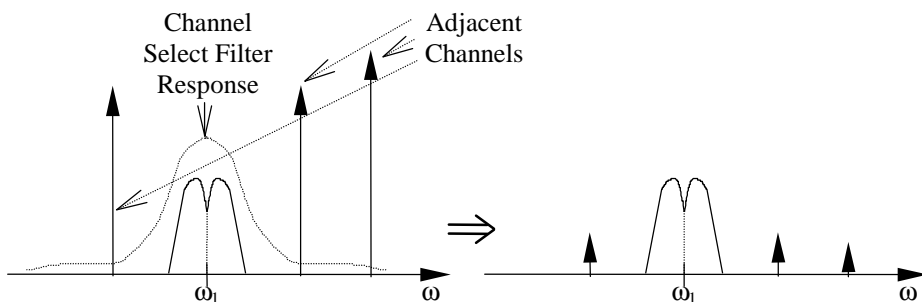


Fig. 3. Problem of channel selection due to finite Q of the channel select filter.

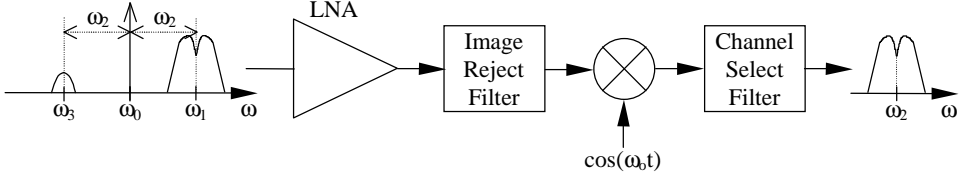


Fig. 4. Simple heterodyne receiver.

easier. An additional benefit of the architecture is that the centre frequency of the channel select filter can be made fixed and different channels can be selected simply by changing the frequency of the local oscillator (ω_0) used for frequency translation.

The frequency translation is made by a process called mixing. In mixing the original signal $v_1(t)$ at frequency ω_1 is translated to a new intermediate frequency (IF) ω_2 by multiplying it in the time domain with another signal $v_{LO}(t)$ at frequency ω_0 . Assuming that the signals are $v_1(t) = A_1 \cos(\omega_1 t)$ and $v_{LO}(t) = A_0 \cos(\omega_0 t)$ and the multiplication is ideal, the following result is obtained with simple trigonometric manipulation:

$$v_2(t) = v_1(t) v_0(t) = A_1 \cos(\omega_1 t) A_0 \cos(\omega_0 t) = \frac{A_1 A_2}{2} \left\{ \cos[(\omega_1 - \omega_0)t] + \cos[(\omega_1 + \omega_0)t] \right\} = \frac{A_1 A_2}{2} \left\{ \cos[(\omega_0 - \omega_1)t] + \cos[(\omega_0 + \omega_1)t] \right\} \quad (2)$$

As can be seen, one half of the power of the original signal is translated to frequency $\omega_1 - \omega_0$ and the other half to frequency $\omega_1 + \omega_0$. Now, one of these multiplication results can be selected by the channel select filter for further processing. Cascading several mixing stages with an appropriate image and channel select filters, the signal can be translated gradually to any frequency. Such receivers are called superheterodyne receivers.

What is the purpose of the image reject filter in Fig. 4.? Suppose we have a desired signal at frequency ω_1 , which is translated to frequency $\omega_2 = \omega_1 - \omega_0$ by a low-side injected local oscillator signal. Now, suppose that there is another signal at the input of the receiver at the so-called image frequency $\omega_3 = \omega_0 - (\omega_1 - \omega_0)$. When this second signal is multiplied with the LO signal, half of the signal power will be translated to frequency $\omega_0 - \omega_3 = \omega_0 - \omega_0 + (\omega_1 - \omega_0) = \omega_2$, which is at the same IF frequency as the desired signal and thus is not rejected by the channel select filter. Therefore, the purpose of the image reject filter, with a much lower quality factor than what the IF filter has, is to filter out the signal at the image frequency before mixing, whereafter it is impossible to separate the desired signal and the image from one another.

While the heterodyne architecture resolves the channel selection problem in a very convenient way, it also brings new complications into the receiver design, such as:

- Trade-off between low Q values of image reject and channel select filters.
- Rejection of signals half way between the LO and signal frequency is problematic due to non-linearities.
- Prefiltering before mixing needed.
- Attenuation caused by the image reject filter lowers the overall noise figure.
- 50 Ω input impedance of the image reject filter loads LNA.
- Two high Q-filters which are hard to integrate.
- Interface between external filters and integrated receiver not optimal (i.e. 50 Ω system).

Because of these problems which lead to size, power consumption and filter realization problems especially in integrated implementations, the designers of radio receivers have been trying to figure out alternative receiver architectures to dispose of the image problem. Image reject, direct conversion, low-IF, wideband-IF and digital sampling architectures are some of these alternative receiver topologies. Of these the architectures based on digital sampling at RF are not studied further, because they are rarely found in current base station receivers.

2.2.2 Image-reject architectures

In order to eradicate the high-quality image reject filter, the architectures shown in Fig. 5. (a) and (b) use arithmetic methods instead to solve the image filtering problem. Let us demonstrate the cancellation of the image using the Hartley image-reject architecture shown in Fig. 5. (a) (Hartley 1928). Let the input signal be $\cos(\omega_1 t) + \cos(\omega_2 t)$, where the signal at frequency ω_1 is the desired signal and the signal at ω_2 is the image. Now after the multiplication with LO signal and writing down only the low-frequency terms present after low-pass filtering, the signals at points A and B are:

$$v_A(t) = -\frac{1}{2} \sin[(\omega_0 - \omega_1)t] + \frac{1}{2} \sin[(\omega_0 - \omega_2)t] \quad \text{and} \quad (3)$$

$$v_B(t) = \frac{1}{2} \cos[(\omega_0 - \omega_1)t] + \frac{1}{2} \cos[(\omega_0 - \omega_2)t]. \quad (4)$$

Now, after the 90° phase shifter (e.g. $\sin(x)$ is transformed to $-\cos(x)$), the signal at point C is:

$$v_C(t) = \frac{1}{2} \cos[(\omega_0 - \omega_1)t] - \frac{1}{2} \cos[(\omega_2 - \omega_0)t]. \quad (5)$$

The sum of the signals $v_B(t)$ and $v_C(t)$ is the final output signal:

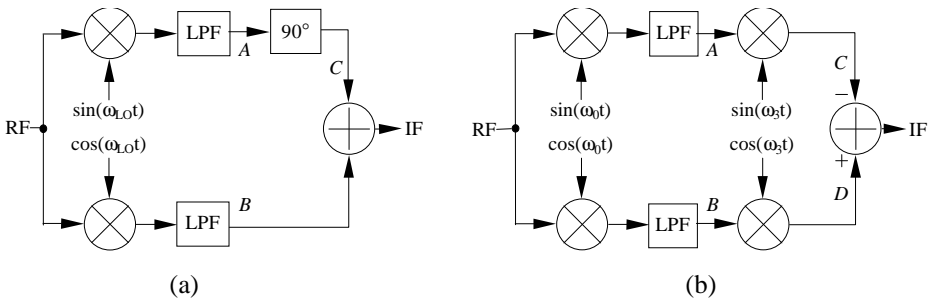


Fig. 5. (a) Hartley and (b) Weaver image-reject receiver.

$$v_C(t) = \cos[(\omega_0 - \omega_1)t]. \quad (6)$$

Thus, the image term has been cancelled in the final addition producing the desired signal as the only output signal for the following IF circuitry.

Having circumvented the need for a highly selective image reject filter, the image reject architectures, like all receiver architectures using quadrature mixing, have their own problems related to the high accuracy requirements of the 90° phase difference and amplitude balance of the two LO signals. The effects of these phase and amplitude errors on the final image rejection ratio ($IRR =$ the ratio of the average power of the desired signal to the average power of the image at the output) of the Hartley architecture have been analyzed briefly by Razavi (1998), for example. Assuming small errors, the net error due to the gain error ε (relative amplitude imbalance) and phase error $\Delta\phi$ (in radians) from the desired 90° can be expressed as

$$IRR_{tot} \approx \frac{4}{(\Delta\phi)^2 + \varepsilon^2}. \quad (7)$$

As can be seen in Fig. 6., where IRR_{tot} is calculated for $0 \leq \Delta\phi \leq 1^\circ$ and $\varepsilon = 0.01\%$, 0.1% , 0.2% , 0.5% and 1.0% , in practice the amplitude imbalance and phase error limit the achievable IRR below some 40 dBc, because it is hard to construct integrated phase shifters with an accuracy better than 1° and amplitude imbalance better than 0.1% . This may lead to the need for additional image filtering or some form of automatic calibration as in Pache et al. (1995).

Since the additional 90° phase shifter in the upper branch of the Hartley architecture in Fig. 5. (a) is often the main source of amplitude error limiting the achievable image rejection, the Weaver architecture shown in Fig. 5. (b) tries to achieve similar image rejection behaviour by producing this 90° phase shift with an additional set of mixers and a secondary quadrature LO signal at ω_3 (Weaver 1956). Thus, the only signal at $\omega_{IF} = \omega_c - \omega_3$ is due to the desired signal, and the image part cancels out at that frequency. An additional low-pass filter is needed after the summer to eradicate the image term at

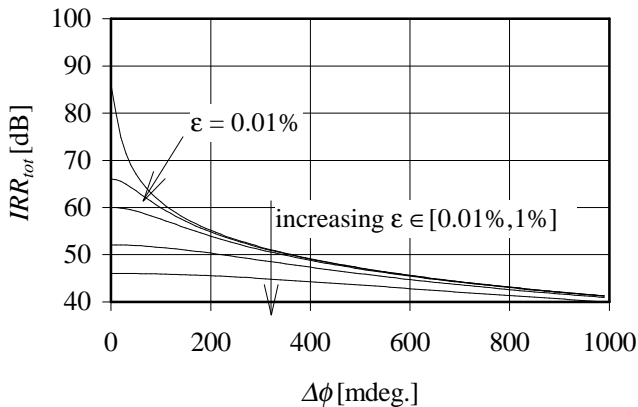


Fig. 6. Image rejection ratio vs. phase error $\Delta\phi$ at various gain errors ε .

$\omega_F + \omega_3$. Another filtering problem may arise if the final IF frequency is non-zero, whereupon an interfering input signal at $2\omega_0 + 2\omega_3 - \omega_I$ will act as an image of the desired signal in the second mixer. If such signals existed in the input, the low-pass filter in Fig. 5. (b) must be replaced with an appropriate bandpass filter. Therefore, as the Weaver architecture removes the additional 90° phase shifter and the amplitude error problem related to it, due to additional mixing, there are new problems associated to the secondary image and to the addition of noisy and possibly power hungry mixers.

2.2.3 Direct conversion or zero-IF or homodyne receiver

The zero-IF receiver tries to make the image reject filter obsolete by making the signal its own image (Tucker 1954, Vance 1982, Abidi 1995, Razavi 1997). The simplest zero-IF architecture suitable for double-sideband AM modulation is shown in Fig. 7. (a) and the more general version for any type of modulation in Fig. 7. (b) (Razavi 1998). In these architectures the incoming signal and the LO signal have the same frequency, thus the multiplication translates the input spectrum directly around DC. The low-pass filters attenuate all unwanted signals outside the desired frequency band.

The zero-IF architecture has several advantages over the conventional heterodyne architecture (Abidi 1995, Razavi 1997, Razavi 1998). A highly selective image reject filter is not required, which will lead to size and power savings. Simpler low-pass filters can replace the bandpass type channel select filter. Additionally, these low-pass filters operate at a very low frequency, which makes them ideal for integration. Since the outputs are around zero hertz, low-frequency amplifiers and analog-to-digital conversion followed by digital signal processing can be used directly after the down conversion.

However, the practical implementation of this promising architecture, especially in an integrated form, with appropriate performance is very difficult. Since the desired signal is converted around DC, the architecture is highly sensitive to all sources of DC power, such as LO self-mixing, LO leakage to antenna disturbing other receivers, re-receiving of the LO signal after reflections from surrounding obstacles, DC offsets in circuit structures and down-mixing of signals due to even order distortion in LNA and mixer (Razavi 1998). Because the signal spectrum is at a low frequency, the $1/f$ noise of active devices becomes a problem. For high IRR, the phase and amplitude balance requirements of the LO signals

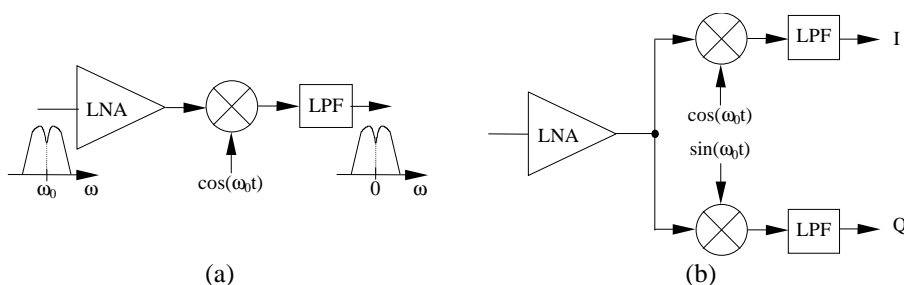


Fig. 7. (a) Homodyne receiver for double-sideband AM modulation and (b) for any modulation.

are tight, as with the image reject architectures. However, a modified architecture called double-quadrature zero-IF promises to reduce this sensitivity somewhat, with the cost of added complexity (Sun & Xu 2000).

The DC offsets degrade the reliability of reception by corrupting the signal and by saturating the following high-gain stages of the receiver. These effects can be reduced by a simple AC coupling which removes the DC offset superimposed on the signal (Schultes et al. 1990, Estabrook & Lusignan 1989) or with a high-pass filter (Takahashi et al. 1992). However, the signal power around DC is also removed by the blocking capacitors or high-pass filter, which may – depending on the modulation type – be unacceptable. Additionally, simple removal of DC cannot reduce the effect of time varying offsets caused by re-received reflections of the LO signal, for example (Razavi 1998).

In some systems the receiver operates only periodically and the idle time can be used for offset cancellation (TDMA). The DC offsets within the receiver can be measured during the idle time and the results used to cancel the offset out during normal operation. The offset cancellation circuitry may be analog (Razavi 1998) or mixed analog-digital, in the case of which the DC value of the incoming signal is calculated digitally for each data slot (Yoshida et al. 1998) or using a short known symbol sequence (Sampei & Feher 1992).

In order to reach the full potential of the zero-IF architecture both the LNA and the mixers should be highly linear to avoid even order distortion. There should be a way to create the well-balanced quadrature LO signals at a high frequency. The isolation between the ports of the mixers should be extremely high. Offsets and $1/f$ noises should be below microvolt level. These design goals are hard to achieve simultaneously, which makes this architecture most suitable for hand-held units, where the quality specifications are not as stringent as in the base station.

2.2.4 Low-IF and wideband IF architecture

The low-IF architecture presented in Fig. 8. tries to combine the good properties of the image reject receiver and the zero-IF architecture (Okanobu et al. 1992, Crols & Steyaert 1995, 1997, 1998). In this architecture the IF frequency is non-zero, yet much lower than in the conventional image reject receiver. The low IF frequency, usually way below 1 MHz, facilitates the use of low-frequency/low-power circuit structures more suitable for integration than the structures of the image reject receiver, yet at the same time it helps to circumvent the DC-offset and $1/f$ noise problems of the zero-IF architecture.

In the low-IF receiver the input signal is first down-converted using I/Q mixing, thus effectively avoiding the image problem (i.e. signal and image do not convert to the same frequency). The image and any other unwanted signals are then attenuated by a complex bandpass filter. A complex bandpass filter is used, because it can have different transfer characteristics for positive (e.g. image) and negative (e.g. signal) frequencies. Such filters can be implemented using analogue or digital techniques or a combination of both (Crols & Steyaert 1995, Behbahani et al. 1999). The complex filtering can also be implemented as part of the $(\Delta\Sigma)$ AD conversion between RF and baseband signal processing (Jantzi et al. 1997). Another variant of the low-IF architecture utilizes high-quality ceramic filters to

suppress the image – the so-called double-low-IF architecture (Banu et al. 1997). The architecture resembles Weaver architecture directly, however, instead of using direct down conversion, like in the original Weaver architecture, the signal is first converted down to a low IF frequency and then up-converted to a suitable secondary IF, where ceramic filters are used for image suppression instead of a complex filter, as in a typical low-IF receiver.

Since in the low-IF receiver the separation between the desired and the image frequency is very small, the image often lies within the system bandwidth and cannot be attenuated by a band select filter. Thus, the image power may be much larger than the signal power (e.g. adjacent channels), which leads to increased image rejection requirements compared to the zero-IF architecture, where the image always has the same power as the desired signal (i.e. the signal is its own image) – a distinctive disadvantage of the low-IF architecture.

For increased image rejection the whole band of interest can first be converted to a lower frequency band, and later mixed down with an additional (double)quadrature mixer. This architecture, called wideband IF or quasi-IF architecture, enables the use of fixed frequency RF mixers and local oscillators in the original down conversion, which makes the realization of highly ideal RF structures convenient. (Gray & Meyer 1995, Rudell et al. 1997.)

The theory of complex signal processing offers an excellent toolbox to describe and analyze receiver architectures (Crols & Steyaert 1995). For example, it is easy to explain using complex notation, what happens in a low-IF receiver. Let us first define some real and complex signals.

$$\sin(\omega t) = \frac{e^{j\omega t} - e^{-j\omega t}}{j2}, \quad \cos(\omega t) = \frac{e^{j\omega t} + e^{-j\omega t}}{2} \quad (8)$$

$$e^{j\omega t} = \cos(\omega t) + j \sin(\omega t) \quad (9)$$

Now, if the lower branch in the architecture shown in Fig. 8. is assumed to represent the imaginary part and the upper branch the real part of a complex valued signal, quadrature down conversion can be expressed as

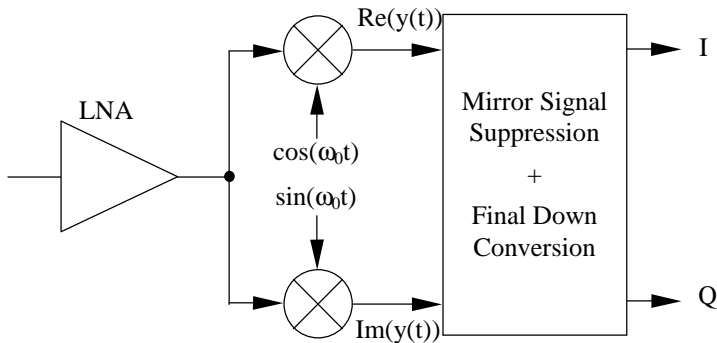


Fig. 8. Low-IF receiver.

$$y(t) = [\cos(\omega_{LO}t) + j \sin(\omega_{LO}t)] \cos(\omega_1 t) = e^{j\omega_{LO}t} \frac{e^{j\omega t} + e^{-j\omega t}}{2}$$

$$= \frac{1}{2} e^{j(\omega_1 + \omega_{LO})t} + \frac{1}{2} e^{j(-\omega_1 + \omega_{LO})t} \quad (10)$$

and after low-pass filtering

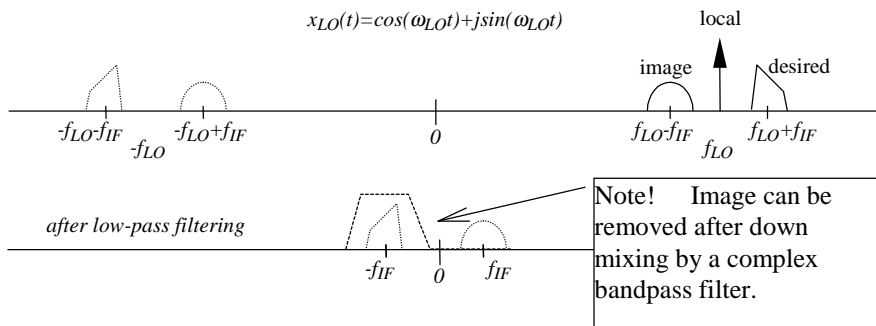
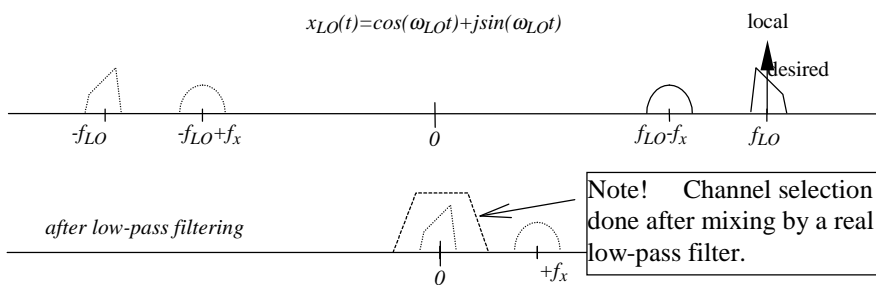
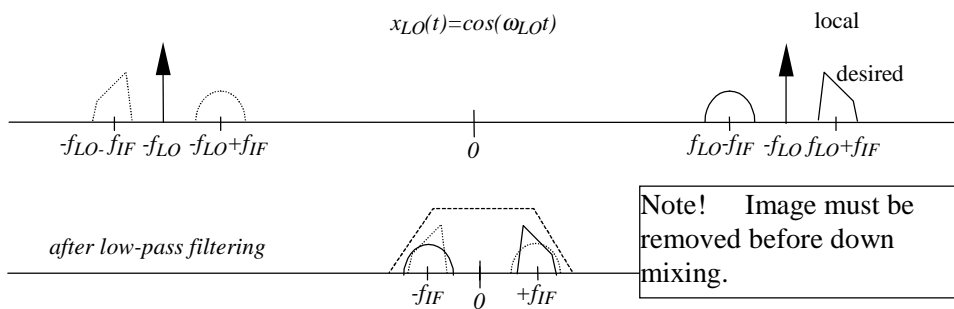


Fig. 9. Principle of the (a) heterodyne, (b) zero-IF and (c) low-IF architecture.

$$y(t) = \frac{1}{2} e^{j(\omega_{LO} - \omega_1)t} = \frac{1}{2} e^{j\omega_{IF}t} = \frac{1}{2} [\cos(\omega_{IF}t) + j\sin(\omega_{IF}t)]. \quad (11)$$

Hence, quadrature down conversion only shifts the negative part of the spectrum of the original input signal to a lower frequency. Therefore, the image and the desired signal do not overlap each other as depicted in Fig. 9. (c). This is also the reason why quadrature down conversion must be used in the zero-IF receiver, when the input spectrum is not symmetrical around the carrier frequency. If a simple mixing were used, the positive and negative frequency components would both translate around DC, where the positive frequency components would act as an image (see Fig. 9 (a) and (b)).

The performance of the low-IF topology is limited by the amplitude and phase imbalance of the complex signal processing. Even if the majority of operations are performed in the digital domain (i.e. perfect complex arithmetic), the accuracy of the quadrature local oscillator limits the image rejection of the complete receiver to the same level with the zero-IF topology. Furthermore, the image rejection requirements of the zero-IF topology are more relaxed, because the level of the image and the level of the signal are always identical, while in the case of low-IF architecture these levels can be significantly different.

2.3 Transmitter topologies

The requirements of the transmitter of a modern telecommunications system are quite different than those of the receiver due to different kinds of signals they process. Contrary to the receiver, the transmitter circuitry processes basically only one signal at a time, the strength and spectral contents of which is well-known. The challenges in transmitter design are thus more related to the spectral purity of the final modulated signal entering the antenna - particularly in systems with many channels closely spaced in frequency any kind of spectral deterioration may disturb adjacent channels. Thus, the performance specifications of transmitters are often given in the form of spectral masks, such as the one in Fig. 10. (Heinen 1998), which takes into account both the ideal spectrum of the modulation method specific to the system and the allowed levels of spurious signals including phase noise, wideband noise and unwanted sidebands. Due to high signal power, the most severe source of spectral deterioration is often the non-linearity of the power amplifier. Therefore, the power amplifier is often made of discrete GaAs devices best suited for such applications, which makes the PA poorly suited for integration with the rest of the transmitter circuitry. Thus, the attention in the following paragraphs is concentrated on the basic transmitter architectures used to realize the required vector modulation and not on the PA. A comparison between the basic architectures is given in Table 1. (Heinen 1998).

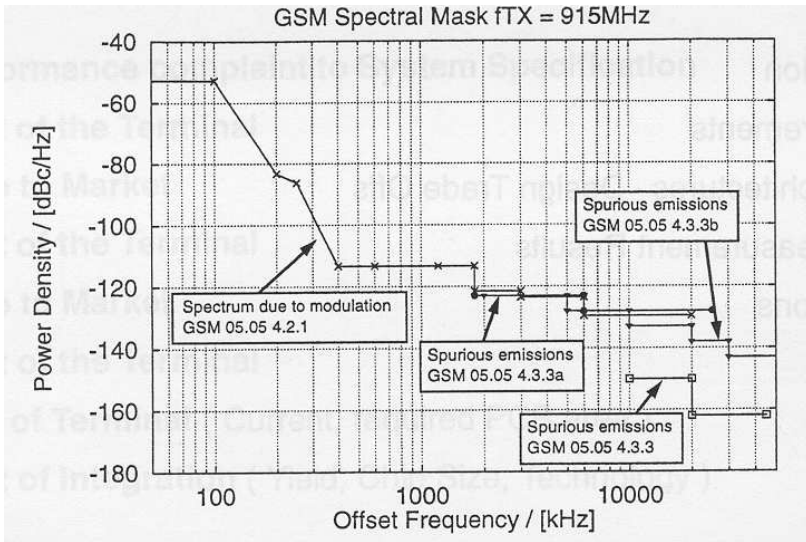


Fig. 10. Spectral requirements of the GSM transmitter.

Direct conversion transmitter, also called the I/Q modulator, shown in Fig. 11. (a) is perhaps the simplest form of vector modulator - excluding the direct modulation of a VCO - and thus very appealing for integration (Razavi 1998, Lee 1998, Heinen 1998, Mole 1998). However, the practical realizations of the simple architecture suffers severely from sensitivity to the imbalance between the mixers and to the phase and amplitude errors between the LO signals. These error mechanisms will lead to increased LO leakage and non-optimal suppression of the image frequency as shown in Fig. 12., where a typical output spectrum of the I/Q modulator with sinusoidal quadrature baseband signals is shown. The LO suppression is strongly related to the imbalance of the mixers and the image rejection to the accuracy of the 90° phase difference between the LO signals. Sensitivity to LO pulling, where the strong output signal of the PA disturbs the operation of the local oscillator, is another shortcoming of this architecture. The sensitivity is high because the LO and the modulated output of the PA are at the same frequency, and gets worse if the PA and the local oscillator are integrated into the same chip. One way to minimize LO pulling is to offset the LO frequency from the output frequency. Offset local oscillators, where two signals are mixed together to produce the final LO frequency, allow the oscillator frequencies and the output frequency to be far away from each other (Stetzler et al. 1995). A similar frequency offset can be generated by doubling the LO

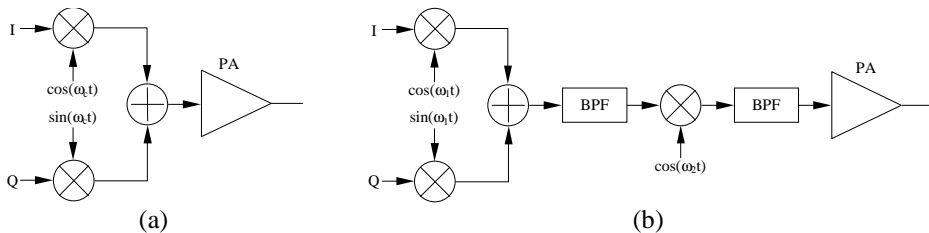


Fig. 11. (a) Direct-conversion transmitter and (b) heterodyne transmitter.

frequency using three-level mixers, for example (Matsuoka & Tsukahara 1999).

LO pulling can also be reduced using the heterodyne structure shown in Fig. 11. (b), where the I/Q modulation is performed first at a lower LO frequency and the final frequency translation by a second mixer stage (Lee 1998). This architecture, also called offset up conversion architecture, can be entirely analogue or the circuitry up to the final up conversion can be purely digital (Meyer & Walters 1990). The architecture offers reduced power consumption, lower wideband noise floor and better image rejection than the direct conversion architecture (Heinen 1998). Additionally, the architecture is well suited for multiband operation, but poor for integration because of excessive amount of high-quality filtering.

A completely different family of transmitter architectures based on the use of phase-locked loops (PLL), which simultaneously circumvent the LO pulling problem and offer a high level of integrability, is shown in Fig. 13. The central purpose of the loop in these architectures is to reduce the phase noise of the VCO and to allow precise channel selection through programmable feedback divider. Since the modulation signal looks like noise from the loop's perspective, the basic problem of these architectures is the attenuation of the modulation spectrum inside the loop bandwidth. Therefore, from the modulation point of view the loop should be of very narrow band, which contradicts spectral purity and frequency switching speed requirements. The simplest PLL based transmitter is shown in Fig. 13. (a), where the baseband signal directly modulates the VCO (Meyers & Walters 1990). One way to reduce the attenuation of the modulating signal at low frequencies is to inject a second modulation related signal to the reference input of the phase detector (Meyers & Walters 1990). Other straightforward ways to bring the modulating signal into the loop are shown in Fig. 13. (b) and (c) (Heinen 1998). Note that the architecture shown in Fig. 13. (c) uses an analogue mixer in the feedback path, thus avoiding the noise enhancement related to the use of digital feedback divider, as in the architecture shown in Fig. 13. (b) (Lee 1998). Actually, this reference modulated transmitter is a close relative to the heterodyne architecture presented earlier - the PLL

Table 1. Comparison of transmitter concepts.

	Direct Modulation	Up conversion Mixing	Modulation Loop
unwanted Emissions RX band	duplexer required	duplexer required	LP-filter + switch possible
Insertion Loss after PA			about 1 dB lower
relative Power Consumption	0	-	+
Dual Band Implementation	complicated	suited	Suited
Major Drawback	not suited for multiband	ceramic filter after up conversion mixer or IMR up conversion	Additional power VCO
Filter efforts	High	high	low

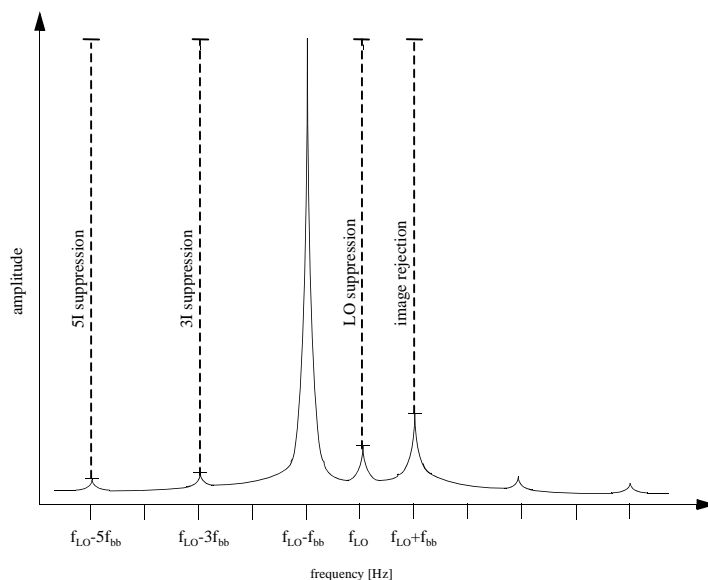


Fig. 12. Typical output spectrum of a direct conversion transmitter.

simply replaces the second bandpass filter.

A very exciting way of imposing the modulating baseband signal on the loop is shown in Fig. 13. (d). The basic fractional-N structure is augmented by a $\Delta\Sigma$ modulator controlling the feedback divider. (Bax & Copeland 1998.) Wideband modulation can easily be accommodated by an equalizer compensating for the effects of the loop bandwidth. The divider control signal could be derived by other methods (e.g. DDS), but the use of $\Delta\Sigma$ modulator adds the benefit of noise shaping.

2.4 Common building blocks in the base station environment

As one contemplates the receiver and transmitter architectures studied in the preceding sections, one can recognize a group of basic RF building blocks found in most of them. Low-noise amplifiers, power amplifiers, synthesizers, mixers and filters are common to all architectures, whether built in a more traditional discrete form or as an integrated circuit. Not all of these basic circuit structures are suitable for integration especially in base station environment where there is no need to trade performance with a smaller area or power consumption. Therefore, the emphasis in the following paragraphs is not in the integration of the whole transceiver circuitry or in the invention of new architectures, but rather in the efficient realization of building blocks fit for integration. This excludes optimised LNA and PA structures using discrete devices and external high-frequency filters. This leaves mixers, especially quadrature mixers specific to vector modulated

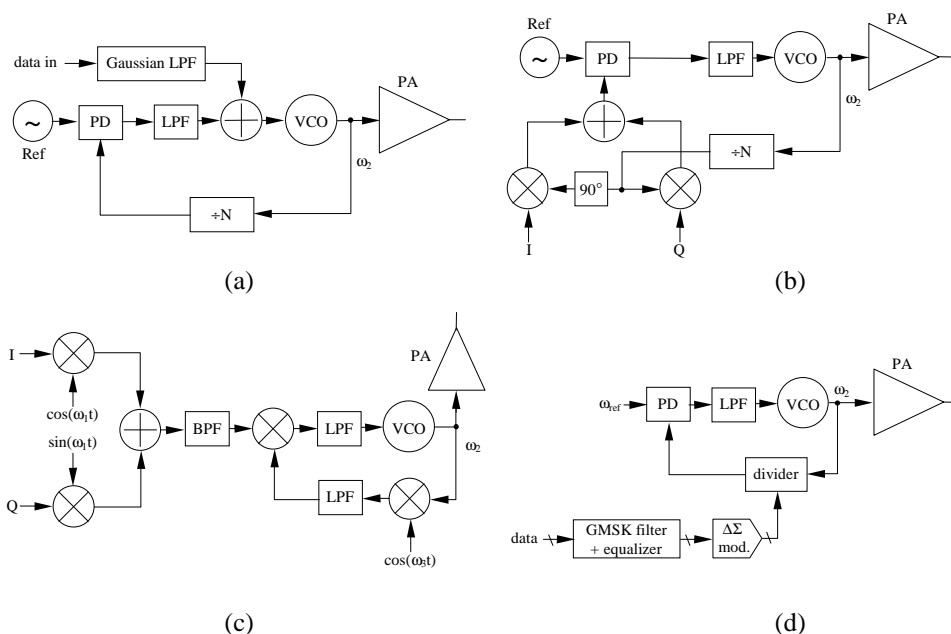


Fig. 13. PLL based transmitter architectures. (a) Direct synthesizer modulation, (b) modulated VCO, (c) modulated reference and (d) $\Delta\Sigma$ feedback modulated transmitter.

systems, and frequency synthesizers that are always present in multichannel systems as the main targets of interest.

2.4.1 I/Q modulator/demodulator

Numerous papers have been published reporting the development of integrated single chip I/Q modulators and demodulators (e.g. Archer et al. 1981, Imai & Kikuchi 1992, Stayert & Roovers 1992, Bóveda et al. 1993, Tsukahara et al. 1996, Borremans & Steyaert 1997, Liu 1998, Matsuoka & Tsukahara 1999). The basic I/Q modulator consists of two mixers driven by two LO signals having 90° differences as was shown in Fig. 11. (a). The quadrature mixers described in the literature introduce a variety of ways to realize the mixer and phase shifter functions.

2.4.1.1 Mixers

Since the mixer is such a crucial part of all RF architectures, the amount of different mixer topologies and their variations is almost endless. In a way the selection of a mixer topology has been made easier as the integration of mixers has become a common daily routine, because only a few mixer topologies seem to dominate the integrated mixer scene nowadays. However, this is only true when one considers the frequency range we are concentrating on in this thesis, that is frequencies around a few GHz. The mixer topologies used at frequencies above some 10 GHz and up to the terahertz range are still

more varied in structure. Due to the extremely high frequencies, these topologies tend to use exotic devices or very simple structures often mimicking those made out of discrete devices, with on-chip inductors, transformers, transmission lines, etc.

Most of the mixer structures used today in integrated mixer applications are based on the so-called Gilbert cell multiplier (Gilbert 1968), the basic form of which is presented in Fig. 14. (a). and the MOS version in Fig. 14. (b) (Razavi 1998). This double balanced differential circuit is highly immune to common mode noise, which makes the cell particularly suitable for mixed mode integration. Actually, the balanced structure has become feasible partly because integration facilitates the use of several relatively well matched active components without problems associated to cost, size and reliability encountered in discrete realizations. A simpler, single-balanced version shown in Fig. 14. (c), is also quite popular in applications where smaller input referred noise is desired and isolation of the LO signal from the mixer output is not critical (Razavi 1998).

If the LO signal operates the two upper differential pairs as ideal current steering switches, the dynamic range and especially the third order intercept point (IP3) of the Gilbert mixer is mainly determined by the properties of the input differential pair. (However, behaviour of the circuit is not this simple, when mismatch and high-frequency effects are considered (Meyer 1986, Coffing & Main 2001)) Then, the output signal is approximately the input voltage signal multiplied by a square wave, transconductance of the input differential pair and the load resistance. Therefore, most of the effort shown in the literature to improve the dynamic range of the Gilbert mixer is spent in finding better input voltage-to-current converters. Contrary to the original one, most of these enhanced input stages try to offer a much lower, ideally purely resistive 50Ω , impedance at the input, because on-chip impedance matching is hard to implement.

Linearization can take a very simple form, as in the case of a simple resistive emitter degeneration. Several differential pairs with offset transfer functions can be connected in

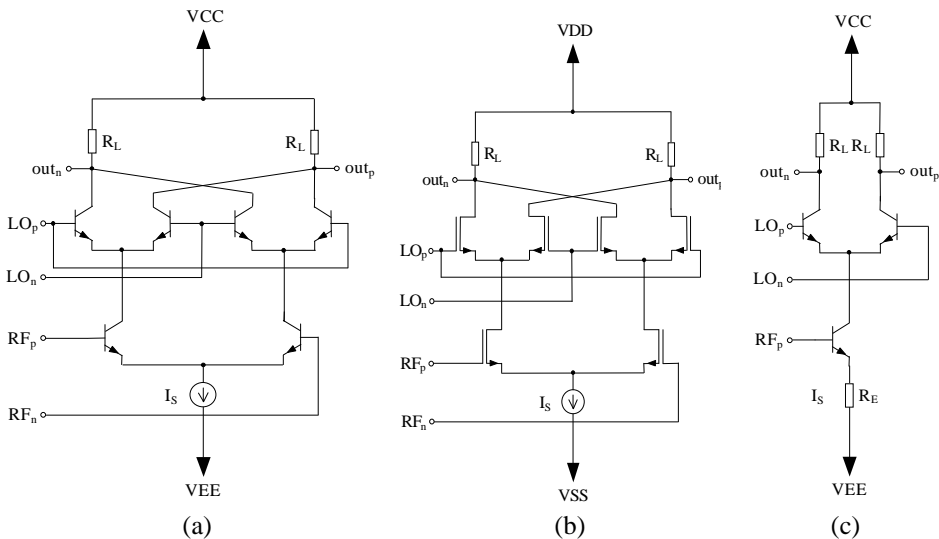


Fig. 14. (a) The basic structure of a Gilbert cell mixer, (b) its CMOS equivalent and (c) the single-balanced version.

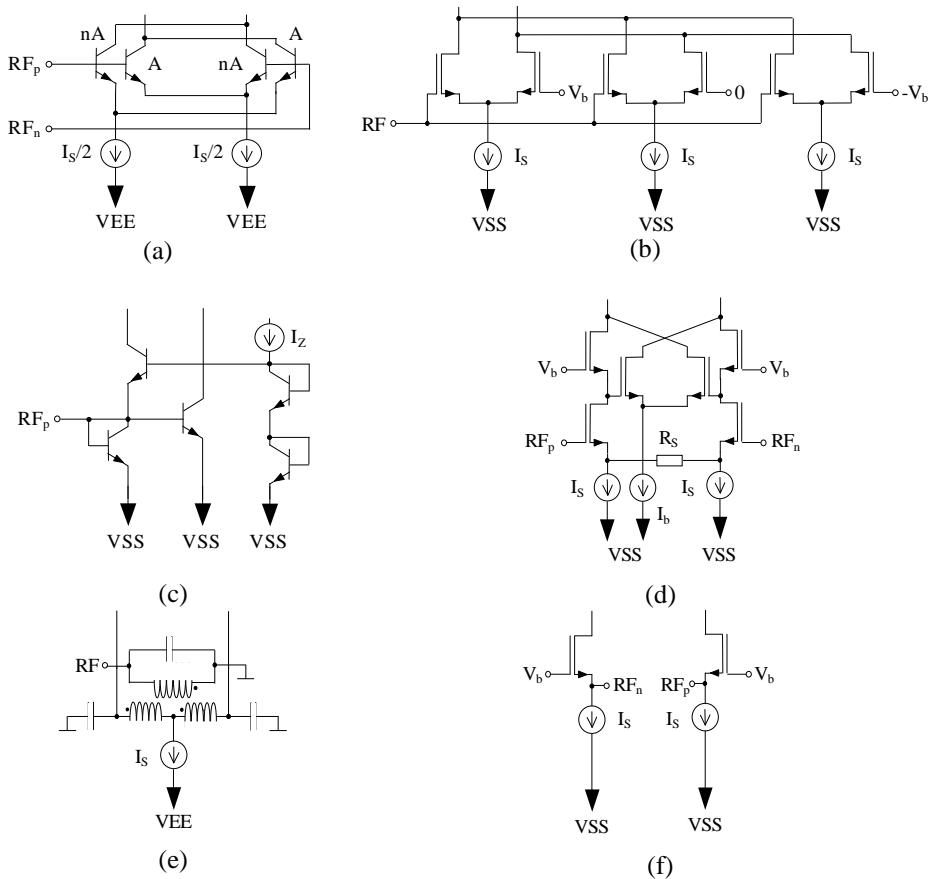


Fig. 15. Various enhanced input transconductance stages.

parallel to form a combined transfer function with a higher dynamic range (Gilbert 1998). In these so-called “multi-tanh” techniques, the transfer functions of the differential pairs can be offset by using transistors of a different size for negative and positive input, as in the Schmoor’s technique shown in Fig. 15. (a) (Gilbert 1998, Razavi 1998), or using a different reference voltage for each input pair as in Fig. 15. (b) (Gilbert 1998, Lee 1998). Unfortunately, resistive degeneration and “multi-tanh” techniques increase the dynamic range by increasing the linearity at the expense of increased noise and reduced transconductance. Additionally, the input impedance is still very high compared to the desired 50Ω .

Due to the above reasons, a very interesting new family of differential class-AB input stages have emerged, which claim to offer superior linearity, good transconductance, single-ended drive, low-power and low-voltage capability, low noise and matching to arbitrary load resistance (Durec 1996, Fong 1997, Gilbert 1997). The transconductance stage of one of these circuits, called the micromixer, is shown in its minimal form in Fig. 15. (c). An excellent paper on this circuit based on the translinear principles (Toumazou

et al. 1990) also reports a more optimal form with additional resistive or inductive degenerations and appropriate PTAT type biasing circuits. (Gilbert 1997.)

Feedback, feedforward and predistortion linearization can take a compact form as in CMOS cascomp transconductor shown in Fig. 15. (d) (Lee 1998) (feedforward), crossquad transconductor (Lee 1998) (positive feedback), current feedback (Behbahani 1997) (negative feedback), true Gilbert multiplier (Gilbert 1968, Lee 1998) (predistortion) or a more complex form requiring several functional building blocks (Ellis 1998) (feedforward). Due to increased circuit complexity, all methods falling to this category tend to increase noise at the expense of increased linearity.

Since the emergence of inductors in increasing number of IC processes, the designers of mixers have turned their attention to circuits utilizing reactive elements for tuned loads, matching, noise minimization and linearization of transconductance. For instance, the use of inductors and transformers in the input stages of mixer cores, like in the transformer based transconductance stage shown in Fig. 15. (e) (Long & Copeland 1995), is attractive, because they are ideally noiseless and linear. In practice, parasitic resistance of inductor wiring and contacts reduces the usability of inductors through added noise. Nevertheless, integrated inductors facilitate the integration of not only new but old, pre-integration era, mixer topologies. Since many of the structures based on, say, transformers and diodes have excellent linearity and noise properties at very low or non-existent supply voltages, they may experience some kind of a renaissance.

Inductors used as loads or for degeneration are not the only way designers have been trying to reduce the high supply voltage requirements of standard Gilbert cell topology due to several stacked transistors. The input pair may be replaced with a grounded-source (Razavi 1998) or common-gate pair stages as shown in Fig. 15. (f), which effectively remove the tail current source(s). In some designs, where LO-to-RF isolation is of special importance, common gate transistors are added to the drains of the grounded-source input pair (Lee 1997). AC coupling (Razavi 1996) and folded current mirrors (Tsukahara et al. 1996, Fraello & Palmisano 1997) have also been used between the transconductance stage and the switching transistors. A convenient way to increase the conversion gain of low-voltage mixers is to inject a suitable amount of extra bias to the drains of the transconductance stage transistors (Schmatz 1995). The same method can be used to reduce the contribution of the shot noise of the switching transistors to the overall noise figure (Razavi 1998).

2.4.1.2 90° phase shifters

The other main building block of the I/Q modulator is the 90° phase shifter needed for the generation of quadrature LO (and possibly in the case of the image reject receiver RF and IF) signals. The accuracy required for the phase shifter depends mainly on the level of image rejection needed to meet the system level specifications – e.g. 35 dB IRR requires $\pm 2^\circ$ phase accuracy (7) – and is limited mainly by processing the variations of component values when integrated phase shifters are considered (Archer et al. 1981, Imai & Kikuchi 1992, Stayert & Roovers 1992, Bóveda et al. 1993, Navid et al. 1997, Shimosava et al. 1998, Matsuoka & Tsukahara 1999). (Amplitude balance is not as big of a problem because some form of signal clipping can usually be performed.) The different phase shifter topologies, some of which are presented in Fig. 16., can roughly be divided into three categories based on filters, digital division or quadrature oscillators.

Simple RC circuits, such as the ones shown in Fig. 16. (a) and (b), may be used as phase shifters, but they have good quadrature accuracy only over a fairly narrow bandwidth and are very sensitive to the variation of resistance and the capacitance of integrated components (Crolls & Stayert 1997). Therefore, some form of balancing, feedback or clipping – amplitude error between the output signals is the dominant source of error – must be performed (Crolls & Stayert 1997, Razavi 1998). A straightforward method for reducing the amplitude error is used in Pache et al. (1995), where an AGC amplifier is used to balance the gains of the two signal paths of a Hartley type image reject receiver. In the presented structure, the phase balance is also improved by distributing the phase shifter between the two signal paths (a low-pass RC filter for one branch and a high-pass RC network for the other). When inductors are available in the circuit process used, low-noise structures based on LC high-pass and low-pass filters, a partial schematic of which is shown in Fig. 16. (d) may be used instead of RC structures (Shimozawa et al. 1998).

Another type of RC circuit shown in Fig. 16. (c) (a two-stage version), namely cascaded sequence asymmetric polyphase filters, is widely used for improved quadrature generation (Crolls & Stayert 1997). When several stages with slightly different centre

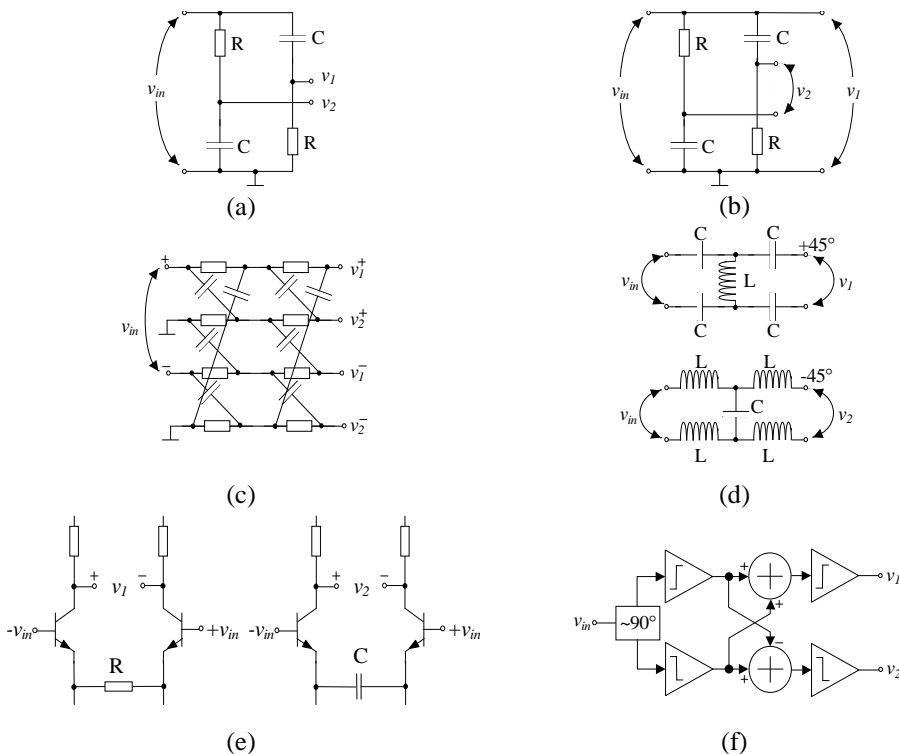


Fig. 16. Different phase shifter circuits. (a) RC high-pass low-pass phase shifter, (b) RC all-pass phase shifter, (c) the sequence asymmetric polyphase filter phase shifter, (d) LC balanced high-pass low-pass phase shifter, (e) phase shifter based on capacitive and resistive emitter degeneration and (f) phase shifter based on Havens amplitude and phase correction circuit.

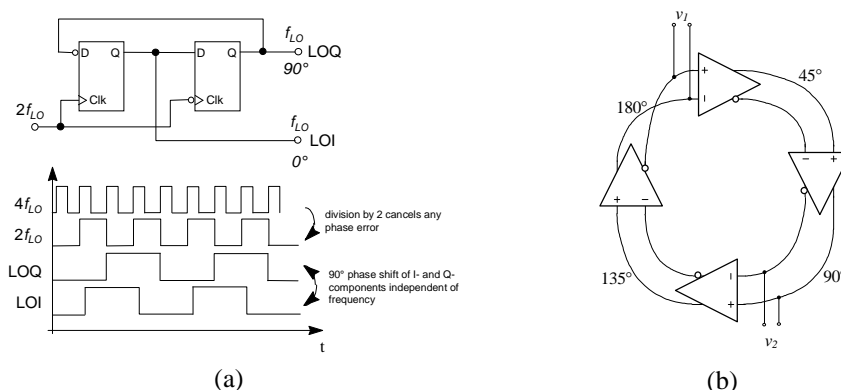


Fig. 17. Phase shifter based on (a) frequency division and (b) on a ring oscillator.

frequencies (centre frequency in this case means the frequency at which the amplitudes of I and Q outputs of a single stage are the same) are cascaded, the amplitude balance of I and Q channels can be made good over a much larger bandwidth compared to the simple RC low-pass high-pass structure described above. In other words, the structure is less sensitive to the absolute values of R_s and C_s – a distinct advantage in an integrated realization, where absolute values can vary tens of percents while the difference between two related values may have an error less than one percent. Cascaded sequence asymmetric polyphase filters are also used to improve the quality of other phase shifters (De Ranter et al. 1999). In these applications the function of the polyphase filter is equivalent to that of the Havens amplitude and phase correction circuit shown in Fig. 16. (f) (Iconomos et al. 1993).

Active devices are often incorporated with RC circuits to form the desired 90° phase shift – a RC all-pass structure working at 1.4 GHz was recently used by Liu (1998), for example. The goal here is to realize gain, produce differential signals and provide isolation from surrounding circuit structures. A straightforward addition of BJTs to a conventional RC structure is used, for example, by Imai & Kikuchi (1992), where BJTs function as simple single-ended-to-differential converters. Simple RC phase shifters can easily be incorporated into conventional amplifier structures. Liu (1998), for example, uses the RC low-pass/high-pass structure at the output of a differential common-base amplifier, thus effectively combining the matched input amplifier and phase shifter into one compact structure. The use of emitter followers for increased driving capability and isolation is evident.

Another kind of analogue phase shifter is presented in Fig. 16. (e), where the phase shift is produced by the difference between the transfer functions of two differential pairs with resistive and capacitive emitted degeneration. The simple and fast structure is used by Stayert & Rooves (1992) and is reported to achieve a phase error of 3° at frequencies from 800 MHz to 1 GHz. This structure will be treated in more detail in Chapter 4. when Paper I is discussed.

A very useful digital phase shifter based on frequency division by two is shown in Fig. 17. (a) (Fenk et al. 1990). This phase shifter operates over a large bandwidth limited by the highest operating frequency of the flip-flops. As long as the incoming clock signal has an accurate 50% duty cycle, the resulting outputs will have a constant 90° phase

difference independent of the frequency. A very convenient way of generating the 50% duty cycle for the input signal is to divide a signal with $f=4f_{LO}$ by two, as depicted in Fig. 17. (a) . However, sometimes circuit operations at twice or four times the final LO frequency cannot be accepted because of the slowness of the process (f_T), feedthrough or power consumption restrictions.

The circuit shown in Fig. 17. (b) uses a ring oscillator to produce the desired LO signals (Matsuoka & Tsukahara 1999). No external LO oscillator is required, and the 90° phase difference is produced by the delays associated with the stages of the oscillator. Consequently, the accuracy of the phase difference between the I and Q signals is directly related to the spread of the stage delays, and the frequency depends on the total delay around the ring, both of which must be well controlled. The control can be automated using a phase-locked loop, for example (Chen et al. 1999).

2.4.2 Synthesizer

2.4.2.1 Introduction

There are various structures based on phase-locked loops and direct digital synthesis that can be used in the base station environment to realize the digital channel selection, synchronization and narrow-band filtering. If used for LO generation and channel selection, the synthesizer must produce adequately low levels of spurious signals and phase noise as well as be sufficiently agile for the given system, because there is only a limited amount of time for the synthesizer to change its output frequency as it moves between channels. The spectral purity of the output signal and the speed of frequency transition are often hard to achieve simultaneously. The advantages and disadvantages of the different synthesizer architectures are summarized in tables 2 through 4 (Noel & Kwasniewski 1994).

The simple integer-N phase-locked loop synthesizer shown in Fig. 18. (a) uses a feedback loop to set the output frequency to a multiple of the reference frequency (Gardner 1979, Best 1997, Rohde 1983). At the same time, due to the filtering performed by the loop, the close-in phase noise of the VCO is attenuated. Thus, the architecture provides two benefits at the same time – it enables the precise selection of the channel frequencies based on the selected feedback ratio N, thus compensating for any drift or random variations between individual VCOs, and attenuation of VCO noise, which would be too large for open loop configuration (i.e. direct control of the VCO). However, the architecture has several problems when used in modern telecommunications systems relating to simultaneous optimization of the speed and spectral purity, for example. Therefore, more advanced loop architectures and direct frequency synthesis methods described below are gaining in popularity. However, the integer-N PLL architecture is still such an important synthesizer architecture and forms the basis for several other loop architectures that it will be discussed in more detail in the next subsection.

To alleviate the problems associated with the integer-N architecture, two integer-N based synthesizers can be used in a dual-loop configuration, such as shown in Fig. 18. (b). The first synthesizer produces a coarse frequency step and the second a small step covering the channels between the steps of the first synthesizer. Speed and reference spur

problems can be avoided, because the first synthesizer uses a high reference frequency – much higher than the channel spacing – and the second synthesizer can be optimized due to its low frequency of operation.

Fractional-N technique shown in Fig. 18. (c) is another means to gain freedom in the selection of the reference frequency and loop bandwidth. The overall N is produced by alternatively dividing the VCO signal by n and $n+1$. This creates, however, a periodic phase error, which produces unwanted harmonics – the main problem associated with this technique. Compensating currents and randomization of the modulus can be used to reduce this problem. The noise power can even be shaped outside the band of interest by randomizing the modulus by a $\Delta\Sigma$ modulator.

The direct digital synthesizer (DDS) shown in Fig. 18. (d) uses an accumulator to address a ROM look-up table the values of which are converted by a digital-to-analogue converter to the final analogue signal. The desired frequency can be selected by varying the increment of the accumulator. Because of its ease of control and speed, DDS is a very prospective way to realize a synthesizer. However, things like the size of the ROM and especially in RF applications, the speed and accuracy requirements of the digital-to-analogue converters are the most severe bottlenecks for its use.

2.4.2.2 Integer-N synthesizer

The cause of many problems associated with the integer-N synthesizer is the equality in channel spacing and the reference frequency. In modern telecommunications systems this easily leads to unacceptable levels of noise and spurious signals at the frequencies of the

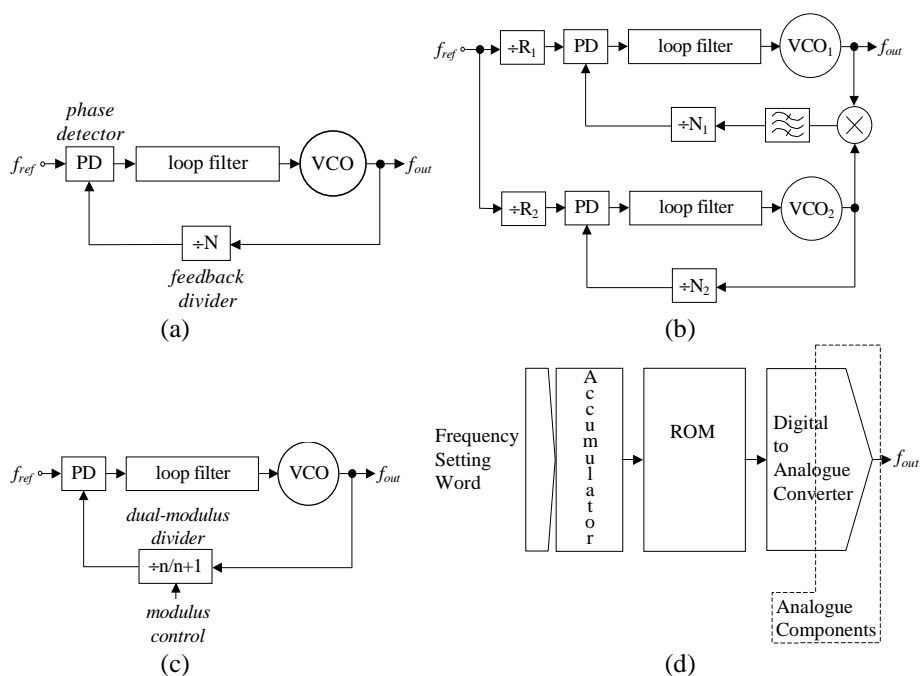


Fig. 18. Basic synthesizer architectures. (a) integer-N PLL synthesizer, (b) dual-loop PLL synthesizer (c) fractional-N PLL synthesizer and (d) direct digital synthesizer.

Table 2. PLL based synthesizer advantages and disadvantages.

Advantages	Disadvantages
- easily configured for complex synthesis via multiloop arrangements, etc.	- expensive
- possible to down-convert input frequency - spacing is increased	- vast amounts of filtering required
- effects of tuned oscillator on stability, accuracy and phase noise of output may be cancelled by the use of a double mixer	- VCO critical to achieving good performance
	- VCO dominates noise away from nominal frequency
	- phase detector design critical
	- lock-up time is related to the smallest frequency component
- phase noise degradation of a signal passing through a filter is possible only if the noise level of the input is very low and if mixers are not optimized	- complex multiple loop synthesis – bulky & expensive
	- coarse tuning steps
	- high phase noise
- useful when spacing between operating frequency is so small that neither passive nor double mix filters can attenuate unwanted harmonics	- random spike and discontinuities
	- spurious effect is severe
	- leakage a problem
	- phase noise modified

adjacent channels when the loop bandwidth is made large enough for fast channel switching. To illustrate this point, the approximate equations for the lock time (T_L) and the noise bandwidth (B_L) of an integer-N PLL using a second order approximation are given as

$$T_L = \frac{-\ln\left(\frac{tol}{f_2 - f_1} \cdot \sqrt{1 - \zeta^2}\right)}{\zeta \cdot \omega_n} \text{ and} \quad (12)$$

$$B_L = \left(\zeta + \frac{1}{4\zeta}\right) \frac{\omega_n}{2}, \quad (13)$$

where ω_n = natural frequency of the loop, ζ = damping factor of the loop, f_i = output frequency before the frequency step, f_2 = output frequency after the frequency step, tol = frequency tolerance and the loop filter is assumed to have a response of the form $(s\tau_2+1)/s\tau_1(s\tau_3+1)$ (Banerjee 1998, Larsson 1995). Consequently, these two quantities are contradictory as one considers the effect of ω_n in the above equations. The conflict is most unpleasant in fast loops, if the phase detector produces signal components at the multiples of the reference frequency – typical for sequential detectors such as the well-known phase-frequency detector described by Crawford (1994), for example – that cannot be attenuated adequately by the LPF response of the loop. These reference spurs, and any non-reference spurs for that matter, will appear at the output spectrum around the carrier frequency, thus disturbing neighbouring channels.

Table 3. Advantages and disadvantages of the fractional-N technique.

Advantages	Disadvantages
- permits synthesis of small frequency increments at a frequency that is an order of magnitude higher than the reference frequency	- currently at technological performance limits
- faster tuning speed	- spurious beat note generated by phase comparator
- possible to generate a jitter free sine wave on the output	- amplitude proportional to comparator gain and rate equal to the rate of the N-1 division
- the average value of the signal moved away from dc making unwanted spurs easier to filter (filter design greatly simplified)	- relatively high FM spurious signals
- becoming a frequency synthesis benchmark	

Assuming a typical phase-frequency detector and charge pump output at the output of the phase detector analyzed by Gardner (1980), for example, the main causes of reference spurs are the leakage of charge from the loop filter and the mismatch between up and down charge pulses of the charge pump at the output of the phase detector (Banerjee 1998, Rhee 1999). For a 3rd order loop Rhee (1999) gives the following equation for the calculation of the 1st reference spur level as a function of phase error ϕ_ϵ :

$$P_r = 20 \log \left(\frac{\sqrt{2} \cdot \frac{I_{cp} R}{2\pi} \cdot \phi_\epsilon \cdot K_{VCO}}{2 \cdot f_{ref}} \right) - 20 \log \left(\frac{f_{ref}}{f_{P1}} \right) [dBc], \quad (14)$$

which in the case of a typical over damped loop can be written as

$$P_r = 20 \log \left(\frac{1}{\sqrt{2}} \cdot \frac{f_{BW}}{f_{ref}} \cdot N \cdot \phi_\epsilon \right) - 20 \log \left(\frac{f_{ref}}{f_{P1}} \right) [dBc], \quad (15)$$

where I_{cp} = magnitude of the output current pulse of the charge pump, R = resistor value of the loop filter, ϕ_ϵ = phase error, K_{VCO} = VCO gain, f_{BW} = loop bandwidth, f_{ref} = reference frequency, N = feedback division value and f_{P1} = frequency of the pole in the loop filter. This equation can be used to estimate the level of spurious signals regardless of the origin of the phase error. The part furthest left in the equation represents the unfiltered spurious signal level caused by ϕ_ϵ and the one furthest right the attenuation provided by the loop filter.

The leakage of loop filter charge during in-lock condition causes the VCO output frequency to drift from the correct value, the effect of which is compensated by the loop by short current pulses replacing the lost charge. Because these very narrow pulses can only appear once for each reference cycle, they have signal components at the multiples

Table 4. Advantages and disadvantages of DDS.

Advantages	Disadvantages
- much faster tuning speed	- D/A performance is a bottleneck
- almost unlimited number of tuning channels	- ratio of D/A settling time:cycle time limiting factor
- phase continuous frequency switching	- D/A differential non-linearity results in transient quantization errors and high-frequency spurs
- efficient modulation facility	- D/A integral nonlinearity results in harmonic dist.
- as inherently frequency stable as the ref. clock	- spurs close to carrier a function of freq., accumulator word size and accuracy of both ROM and D/A
- very high tuning range	- fast D/A converter difficult to make accurately
- low phase noise dependent on D/A quantization	- discrete narrowband spurs
- numeric frequency tuning	- reference source must operate at a higher frequency than that synthesized
- tuning speed restricted to 2 or 3 clock cycles	- relatively high power consumption
- very high frequency resolution	- generally confined to low-frequency signals
- excellent long & short term stability	- FHSS – phase quantization noise problem
- highly linear frequency tuning	- amplitude quantization causes degradation
- good amplitude response	- not very power efficient
- sub-microsecond setup time	
- multioctave operation	
- phase coherent frequency changes	
- low cost and low complexity	
- relaxed shielding requirements	
- requires no alignment	

of the reference frequency up to a very high frequency. The phase error caused by leakage can be expressed as (Rhee 1999):

$$\phi_e = 2\pi \cdot \frac{I_{leak}}{I_{cp}} [rad], \quad (16)$$

where I_{leak} is the total leakage current to the charge pump, VCO and any other leakage mechanisms and I_{cp} is the magnitude of the output current pulse of the charge pump. Obviously any phenomenon increasing leakage (e.g. increasing temperature and higher VCO control voltage (Banerjee 1998)) will increase the level of spurious signals. If equation (16) is used in equation (14), it can be seen that leakage is more serious in loops with a lower reference frequency and high VCO gain. At low reference frequencies there is more time for the leakage current to flow between correction pulses from the phase detector, thus making the pulse wider and increasing the signal power at multiples of the reference frequency. Clearly, a higher VCO gain will increase the level of spurious signals because small variation in VCO control voltage due to leakage and the correction pulses gets amplified by K_{VCO} .

Another cause for reference related spurious signals dominating in applications having high reference frequencies is the mismatch of the current levels of the up and down current pulses coming from the phase-frequency detector. The difference of these current levels makes a small repeating current pulse appear at the output of the charge pump, when the zero output is produced as the sum of the sink and source currents. The magnitude of the phase error caused by mismatch can be expressed as (Rhee 1999):

$$|\phi_\varepsilon| = 2\pi \cdot \frac{\Delta t_{on}}{T_{ref}} \cdot \frac{\Delta i}{I}, \quad (17)$$

where Δt_{on} = the turn-on time of the PFD or the minimum pulse width to avoid dead-zone, T_{ref} = reference period, Δi = mismatch of the current levels and I = current pulse magnitude. Due to the finite output impedance of the UP and DOWN current sources, the mismatch is a function of the voltage at the output of the charge pump. A more general form for equation (17) expresses the phase error not as a function of current differences but of charge differences, thus accounting for other mismatch mechanisms. A typical source of charge mismatch is the different turn-on times of PMOS and NMOS switches used in the charge pump circuitry and delay mismatches associated with the PFD itself (Rhee 1999). Thus, often the optimum spurious performance is not reached when source and sink currents are exactly the same but slightly different, thus compensating for the effects of the secondary mismatch sources (Banerjee 1998).

Another problem caused by equal reference frequency and channel spacing happens if the output frequency is much higher than the reference frequency, thus leading to a very large feedback divider ratio N . This leads to increased output phase noise, since noise originating from all other loop components except the VCO get multiplied by N . To see this more clearly, the phase-noise transfer functions for different noise sources are summarized in Table 5 and, furthermore, the transfer functions $T_0(s)$ and $T_{VCO}(s)$ can be written as (Banerjee 1998):

$$T_0(s) = \frac{G(s)}{1 + G(s) \cdot H} \approx \begin{cases} N, \omega \ll \omega_c \\ G(s), \omega \gg \omega_c \end{cases} \text{ and} \quad (18)$$

Table 5. Transfer functions of different noise sources in the PLL loop.

Source	Transfer Function
Crystal Reference	$\frac{1}{R} \cdot T_0(s)$
Reference Divider	$T_0(s)$
N Divider	$T_0(s)$
Phase Detector	$\frac{1}{K_D} \cdot T_0(s)$
VCO	$T_{VCO}(s)$

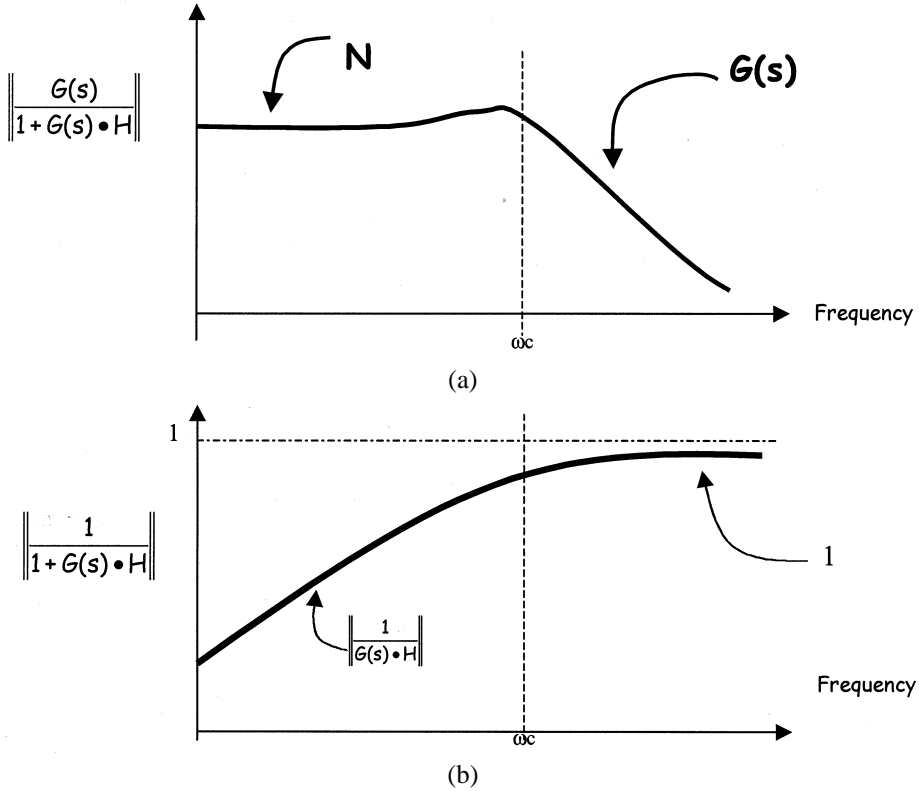


Fig. 19. PLL noise transfer functions (a) $T_{\theta}(s)$ and (b) $T_{VCO}(s)$.

$$T_{VCO}(s) = \frac{1}{1 + G(s) \cdot H} \approx \begin{cases} \frac{N}{G(s)} & , \omega \ll \omega_c \\ 1 & , \omega \gg \omega_c \end{cases} \quad (19)$$

where $H = I/N$, N = feedback divider ratio, R = reference divider ratio, $G(s)$ = open-loop gain = $K_D K_V F(s)/s$, K_D = PD gain, K_V = VCO gain, $F(s)$ = transfer function of the loop filter and ω_c = loop bandwidth. The position of the corner frequency ω_c is illustrated in Fig. 19., where the above transfer functions are sketched (Banerjee 1998). Now, the effect of large N on phase noise is clearly seen in Fig. 19. (a) since all noise sources except the VCO will be multiplied by N at frequencies close to the final output frequency. Contrary to this, as shown in Fig. 19. (b), the noise originating from the VCO will be attenuated within the closed loop bandwidth – one of the major benefits of PLL type synthesizers.

Even with its various problems, the traditional integer- N frequency synthesizer is still commonly used in the base station environment. Because the size and power restrictions are relaxed, the synthesizer circuitry can be optimized with high-quality VCOs and loop filters made of discrete components, and even parallel structures. The so-called ping-pong synthesizer, for example, uses two complete integer- N PLL based synthesizers in parallel.

While one synthesizer is producing the final output signal, the other is allowed to change its frequency slowly, effectively facilitating the separate optimization of spurious and speed properties of the complete synthesizer. Thus, from the base station point of view, the parts of the loop appropriate for integration are shown in Fig. 20. inside the rectangle labelled 'PLL IC'. The VCO remains external, because a discrete one has superior spectral properties due to better-quality reactive components, optimal choice of transistor technology and better isolation. The external loop filter makes the design easily customizable for different applications. Fig. 20. also highlights other typical features of the base station synthesizer. As shown, a second order current driven passive integrator is often used, because it offers high suppression of reference related harmonics with low noise and without the use of an op-amp. A notch in the frequency response of the loop filter attenuates the first reference harmonics, which is usually the largest. Due to the type of the loop filter, the PFD has a current type output.

The loop environment poses challenging requirements for the charge pump circuitry. The charge pump must have low current noise at its output (SNR typically above $150 \text{ dB}/\sqrt{\text{Hz}}$), since it is magnified in the loop by a factor relative to the feedback divider N – see equation (19). For minimum reference related spurs, the charge pump must provide precisely matched source and sink current, especially if zero output is formed by the sum of these currents. For optimum current balance the sources must have a very high output impedance, because the DC voltage at the output varies with the VCO frequency. Disturbances in the absolute and relative magnitudes of the source and sink currents will lead to changes in the gain of the phase detector and in the levels of the reference spurs in the output spectrum, as was explained above.

The main emphasis in recent research related to the integer- N type PLL synthesizer seems to be on finding ways to speed up the frequency transition of the synthesizer without compromising the purity of the synthesized signal. These methods allow the closed-loop bandwidth of the loop to be low for added suppression of the reference related harmonics and RMS phase-noise without making the loop too slow for fast frequency switching. This can be done with improved loop components or by architectural modifications. Either way, the operation of the loop is in some cases affected only during the frequency transient and in other cases also during the normal, stable, operation.

A pre-tune signal temporarily superimposed on the loop filter can be used to bring the output frequency closer to the desired new value, thus making the frequency transition faster. A feed-forward system can be used (Zhang & Allen 1999) or a simple voltage ramp may be added to the output of the loop filter (El-Ela 1999). Modulation of the output current level of the phase detector can be used to enhance the transient behaviour of the charge pump PLL during frequency hop (Hati & Sarkar 1999).

A similar effect is generated by a nonlinear phase detector, the gain of which grows with increasing phase error (Larsson 1995). Another way to realize a nonlinear phase detector characteristic is to use adaptive bandwidth control, which automatically controls the loop bandwidth according to the locking status and the phase error amount (Lee & Kim 2000).

The phase comparison frequency can be increased using a digital phase accumulator as the phase detector, thus allowing the use of a higher closed loop bandwidth (Efstathiou et al. 1996). A similar effect is achieved, if parallel phase detectors with delayed reference

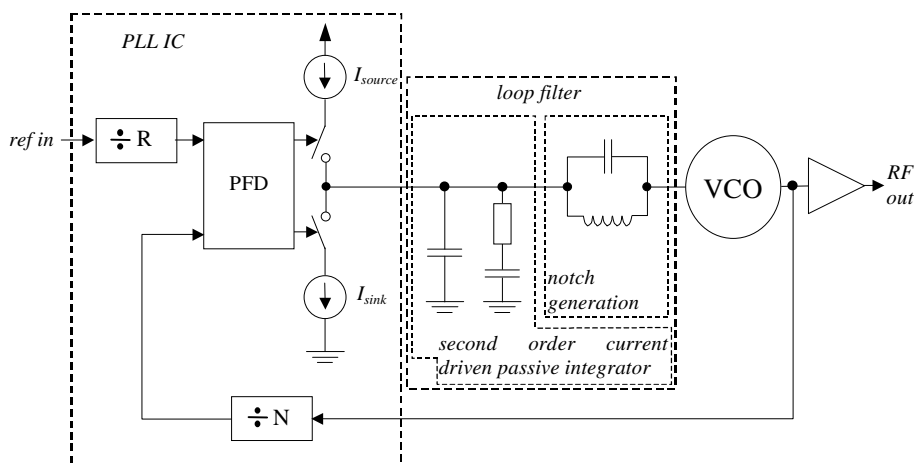


Fig. 20. Structure of a typical base station synthesizer.

signals (Sumi et al. 1998, 1999) or operating at multiples of the reference frequency (Park & Mori 1991) are used, thus performing phase comparison several times during one reference cycle. If the output frequency transition has peaking, a frequency detector may be used to catch the first occurrence of the final output frequency. The transition can be made fast by switching the output charge pump constantly to the source or sink mode. (Sumi et al. 1997.)

The loop can be made faster during frequency hop by changing the values of the loop filter components (Adachi et al. 1995, Sumi et al. 1997). For enhanced effect, the loop gain can also be increased for the duration of the hop giving a two-mode pull-in technique (Sato et al. 1992). Similar techniques (often called Fastlock or something similar), where the output current of the charge pump and one loop filter resistor are switched are used also in some commercial synthesizer ICs (IntersilTM 2000, National SemiconductorTM 1997).

Simple accumulators can be used as a phase detector with increased phase comparison range, thus avoiding any cycle slips which effectively slow the loop down (Brennan 1996), or a numerical phase comparator with a digital loop filter can be used to avoid large time constants of an analog loop filter (Kokubo et al. 1995). If DSP is used to derive the VCO control signal by the subtraction of the reference phase and the feedback phase, no band limiting loop filter is needed at all (Kajihara & Nakagawa 1989, Kajiwara & Nakagawa 1992a, Kajiwara & Nakagawa 1992b). A very interesting way to realize a complete RF synthesizer using a single readily available DSP IC, analogue loop filter and off-chip VCO is presented by Zuta (1998). This design is based on the use of DSP counters and adders which allow phase comparison in a more continuous fashion (i.e. phase comparison is performed many times during one reference cycle by comparing the contents of the reference and feedback counters).

One phase-locked loop can be used to control two VCOs with sample and hold circuits at their input (Mizogushi & Seki 1995). The loop is used to find the precise input voltage of the VCOs for a given frequency, after which the voltage is held constant by the sample and hold circuit. While the other VCO is producing the final output frequency in an open-loop configuration, the other VCO operating inside the loop has plenty of time to reach

the new frequency. Whilst the use of a free running VCO avoids reference spur problems, it necessitates the use of a very low phase noise VCO.

Techniques approaching fractional-N techniques have also been reported. N-stage serial (Park & Mori 1992, Saba et al. 1993) or parallel (Saba et al. 1994, Saba et al. 1995) cycle swallowers have been used between the VCO and the feedback divider to make the reference frequency and the smallest output frequency step independent of each other.

Vaucher (2000) reports a way to circumvent the contradiction between the settling time and spurious problems by applying an adaptive tuning system. This architecture uses two phase detectors one of which is optimized for in-lock operation (i.e. spurious attenuation and low noise) and the other for fast channel switching. The PD enabling fast frequency switching only operates during channel switching, thus in effect enabling the separate optimization of in-lock and transient operations.

An interesting way to reduce the level of spurious signals by lowering the gain of the VCO is suggested by Lin & Kaiser (2000). In this approach the complete tuning range of the VCO is broken into discrete overlapping tuning ranges. Each tuning range can now be realized with a smaller K_{VCO} , thus reducing the level of reference spurs as shown in equation (14). The discrete tuning ranges are generated using rather complex SC techniques with an auxiliary coarse tuning loop and CMOS varactors. A quite similar structure is also reported by Lo & Luong. (2000).

The main shortcoming of many of the speed-up methods presented above is the fact that they require changes to be made not only to the architecture, but also to the individual building blocks of the synthesizer. Consequently, their application to existing synthesizer designs is not an easy task. This is especially true, if the synthesizer is partly integrated. However, in many such applications, the loop filter is left outside the synthesizer IC allowing the properties of the PLL to be tailored for different applications. Therefore, in Chapter 5 a speed-up method which does not require re-designing existing synthesizers is proposed. The method is based on using charge pulses to control the dynamics of the loop and only requires access to the loop filter.

3 Practical RF-IC Design

The design of RF-ICs for the base station environment does not differ much from any high-frequency IC design. Maybe the one single thing that makes the base station environment different from the IC designer's point of view, is the relaxed power consumption specifications. Thus the designer can more freely optimize the performance of circuit structures to meet speed (i.e. optimization of the f_t of individual transistors), distortion and matching specifications. Otherwise the following paragraphs deal mostly with common problems in any analogue high-frequency IC design.

The basic design flow is depicted in Fig. 21. (Rein & Möller 1996). The target specifications usually come from the customer or from system level requirements and, thus, it is the designer's key task to produce a design meeting those specs. Before the final circuit design and simulation, the designer also has to choose a suitable technology to realize the circuit or circuit block. Often, the designer has to cope with a given process already chosen according to the requirements of other circuit functions (e.g. mixed mode circuits prefer CMOS processes), prize and availability (companies often require several process vendors providing similar processes for reduced risk). Thus, for the designer, who does not usually have the opportunity to refine the models of circuit elements (usually

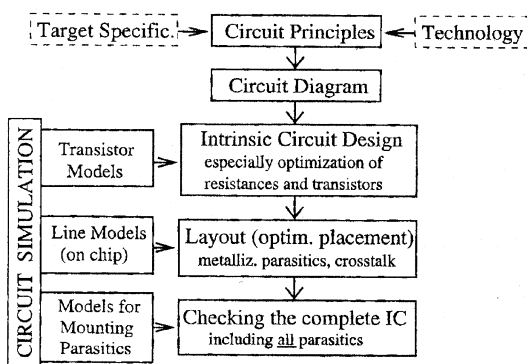


Fig. 21. Basic steps in the design of high-speed circuits. For simplification the iteration loops between the different steps are not shown.

done by the process vendor), the rest of the design process means going back and forth between the design steps shown on the right in the diagram. The design flow is by no means a one-way process, but often requires several iterations even all the way from the bottom of the diagram to the top.

The design of RF-ICs is especially difficult if the circuit process is not optimum for RF circuit functions. This fact is especially pronounced in mixed signal design in CMOS, where the process may be particularly optimized for digital circuitry. Due to its smaller share in the overall electronics industry, analogue electronics has not been a driving force behind the development of processing technology in a similar manner as digital electronics (e.g. microprocessors, memories etc.). Even if a process happens to be well suited for analogue design, cost and risk factors usually force the designer to use well established processes, where the maximum operating frequency is close to the signal frequencies of the RF part of the circuitry. Thus, the designer is forced to clever circuit techniques, and innovative topologies to push the speed limits.

Working at high frequencies and near the capabilities of the process make circuits strongly sensitive to component parasitics and modelling errors, which makes manual analysis hard even with moderate accuracy. Thus, the designer must rely heavily on circuit simulation for fine-tuning of the circuit properties. Even this approach does not always lead to successful design because of the inaccurate device and parasitic models. The use of circuit simulators as design aid is further hindered by the increasing size of circuits and the huge difference in signal frequencies between the RF part and the baseband part of a complex RF-IC – large end time value necessitated by the low-frequency baseband signals and a small time step necessitated by the fastest RF signal produce a huge number of simulation points in a typical transient analysis in SPICE type simulators – which both lead to long simulation times. Also, the numerical accuracy of simulators may be inadequate for the simulation of circuits with an extremely large dynamic range, at least with default simulator options (Avant! 1998). Unfortunately, increased accuracy will also increase the simulation time. Since the simulation time of a complete mixed-mode IC, such as synthesizers using SPICE type simulators can easily extend to days, a so-called mixed-mode simulation must often be used, where the digital parts of the circuit are simulated using a logic simulator, thus effectively trading accuracy for speed.

Analogue circuit structures working at RF frequencies are highly sensitive to layout related design issues. Layout parasitics such as capacitance between the wiring and the substrate and the capacitance between wires cause changes in the circuit response, mismatch between the branches of differential circuit structures and signal crosstalk between circuit blocks. The performance of a circuit block, e.g. the LO suppression of an I/Q mixer or the accuracy of phase shifters, can deteriorate unacceptably low due to device mismatch. Adjacent circuit blocks, both high-frequency and baseband circuitry, can disturb other circuit functions through crosstalk via the substrate, inductive cross coupling between bonding wires and noise induced to the internal power lines due to the common bond wire inductance (i.e. ground bounce). A comprehensive list of references about crosstalk related matters can be found in Clément (2000).

The parasitic effects can be minimized to a certain degree through extensive yield analysis and careful layout design. Statistical simulations, both corner analysis and Monte Carlo type, can be used to maximize the number of working circuits between subsequent fabrication runs. Parasitic extraction from the layout for accurate circuit simulation can be

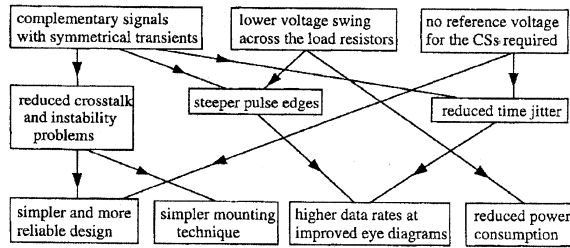


Fig. 22. Advantages of differential operation (compared to single-ended operation).

used to avoid some of the effects caused by wiring capacitances. Unfortunately, today such an extraction does not usually include the effects of capacitive coupling between wiring and the substrate coupling. Therefore, as of now, the designer must mainly rely on his or her design expertise and good design practice to avoid these effects without the means to check the effectiveness of the chosen approach or to optimize the design in this respect. Thus, common centroid structures, large devices and so-called dummy devices are often used (Johns & Martin 1997). Depending on the type of the substrate, sensitive circuit blocks can be shielded from noisy parts of the chip by different guard structures (Clément 2000). One widely used design practice to minimize some of the problems described is the use of differential signals and structures inside the integrated circuit. Some of the benefits of differential circuitry are summarized in Fig. 22. (Rein & Möller 1996).

Due to the high-frequency of operation, the packaging of the RF-IC must be considered carefully in order to avoid the deterioration of circuit properties due to parasitics. Several packaging methods, such as wire bonding, flip chip, multi-chip modules and chip scale packaging, offering different cost, size, parasitic and crosstalk properties are available (Lin 1998). Using advanced packaging, such as the flip chip technology shown in Fig. 23. (a), most of the parasitics of traditional wire bonding can be avoided. For example, the effective inductance due to the bond wire – a major parasitic when connecting the chip to the outside world – can be dramatically reduced and thus circuit operation at higher frequencies guaranteed (see Fig. 23. (b)).

Today, however, it is still quite typical to use normal wire bonding to package base station RF-ICs into a circuit package, thus a few more words about this type of packaging is in place. For an optimum wire bond, the chip should be bonded using as short wires as

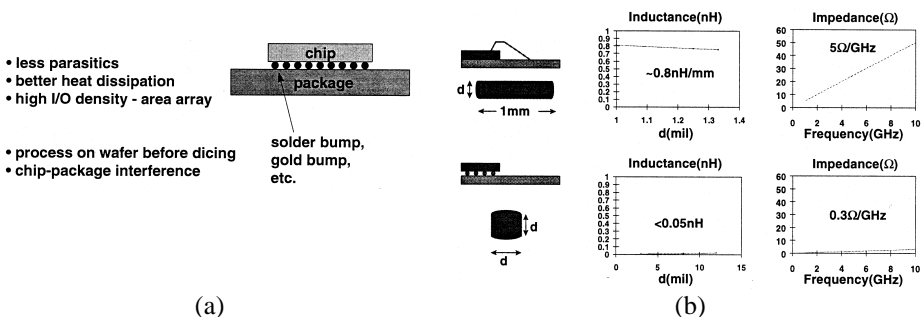


Fig. 23. (a) Flip chip technology and (b) comparison between flip chip and wire bond parasitics (Lin 1998).

possible. Thus, a package with a minimum size cavity for the chip should be selected. If possible, the chip should be oriented and mounted into the cavity in such a way that the bonding pads of the highest frequency inputs are placed near the cavity edge. The parasitics caused by the lead frame and pins must also be minimized through the selection of a proper package type (e.g. SOIC). In order to keep the package size small (small package gives smaller parasitics), the number of pins needed should be as small as possible.

The package manufacturers have recognized the importance of package and bond wire inductance by providing the designer with complex schematic level models of their products. An example package and bond wire model for one bond wire is shown in Fig. 24. The model takes into account the parasitics caused by the on-chip bonding pad, bond wire, lead frame and pins. Note that also the cross coupling via mutual inductances and parasitic capacitances is included for added accuracy. Unfortunately, a complete model of a, say, 28 pin package consists of a large number of elements, which increase simulation time considerably – especially the resonance effects caused by the presence of inductive elements require the simulator to take extremely small time steps during simulation. Thus, often accurate package models are only used at the high-frequency inputs.

Some design principles commonly used by RF-IC designers after choosing a circuit package are discussed next. The cross coupling of signals via the supply lines can be reduced by dedicating each sensitive circuit structure with its own supply pins (and bonding wires). Signals which must be isolated from each other, are usually brought to the circuit perpendicularly to minimize inductive coupling. Differential signals, on the other hand, should be brought in using adjacent bonding wires. In that case the mutual inductance helps to reduce the overall inductance seen by the input signals. In addition, the inductance of bonding wires is often reduced by using several bonding wires in parallel. Some packages offer the so-called hard ground pins which can be used to ground the chip's bottom exceptionally well and thus help to reduce substrate coupling in some cases (the benefit depends on the type of the substrate (Clément 2000)).

The importance of accurate package modelling leads to a modified RF-IC design cycle presented in Fig. 25. (Lin 1998). This so-called package circuit co-design methodology adds the package modelling to the flow diagram shown earlier in Fig. 21. As shown, the package models, provided by the manufacturer or custom made using EM simulation, should be included in the simulations as early as possible in the design cycle.

Unfortunately, no matter how carefully an IC is designed, there will always be circuits

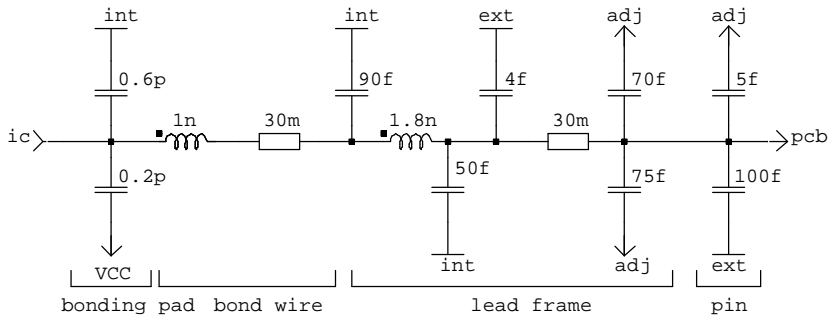


Fig. 24. Example packaging model of a SOIC type package including the parasitics due to bonding pad, bond wire, lead frame and pins.

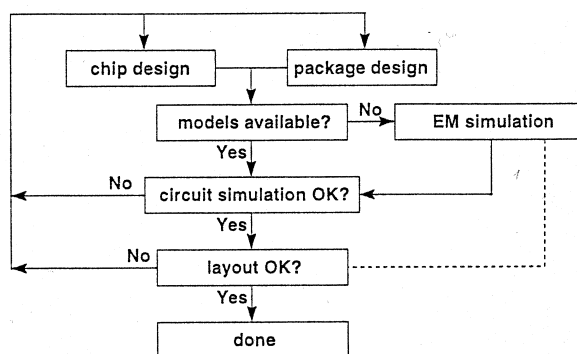


Fig. 25. Circuit-package co-design flow chart (Lin 1998).

that do not work after fabrication. In cases like that it is very important for one to be able to pinpoint the source of the problem within a circuit. This process usually requires the characterization of individual circuit blocks, which is not easily possible since the packaged circuit does not offer access to all nodes of the circuit. Thus, it is a good practice, at least in experimental circuits, to provide access to additional nodes for testing and characterization purposes. Even with a perfectly functioning chip the possibility to characterize individual circuit blocks can provide information valuable for future designs (e.g. reuse of circuit structures).

One quite convenient way to add flexibility to the circuit testing is to add probing pads to the layout of the circuit during design. This can, however, be done only if the parasitic capacitance of the quite large area of metal (e.g. $50\mu \times 50\mu$) does not change the operation of the circuit too much. To minimize the parasitic effects caused by the parasitics to the balance of differential structures, the pads should be added to both differential arms, even if only one is actually used. The size of the needed probing pads depends heavily on the type of probes used. The probing of both low-frequency and high-frequency signals can be accommodated either by simple square type low-frequency pads suitable for needle type probes or differential pads suitable for high-frequency differential measurements (Cascade 2001). As an example, such probing pads were used in the circuit described in paper III, the layout of which is shown in Fig. 26. (a). The additional pads shown enable the characterization of the three major blocks (variable gain amplifier, fixed gain amplifier and output buffer), since they grant access to all inputs and outputs of the blocks.

Some design errors can nowadays be corrected after fabrication using advanced layout tooling (LaserProbe 2001). Thus, wires may be cut and new ones grown to correct errors or to bypass circuit structures as shown in Fig. 26. (b). Probing pads (mainly for needle type probes) can be grown and connected to almost any node. These methods can also be used not only to mend circuit problems but also to cut out parts of the chip used for characterization purposes after characterization is done as in Paper I.

Since the impedance matching between circuit blocks at high frequencies has a strong influence on the overall performance of the RF system, the designer of RF-ICs must be familiar with RF theory and the system around his or her circuit during initial circuit design to be able to optimize the interface between IC and the final operating environment. Due to the small dimensions within an integrated circuit and narrowband

4 Description of the developed circuits and the main results

4.1 I/Q modulator circuits

Two I/Q modulators for the direct conversion transmitter architecture in the GSM base station (carrier frequency ~ 1 GHz) are described in papers I, IV and V. Papers I and IV discuss the respective modulators and paper V attempts to compare their performance to each other and to various other similar circuits reported in the literature. Even though the papers focus on the direct conversion transmitter, the RF amplifiers, 90° phase shifters and Gilbert multipliers described could be used with minor modifications in any transceiver architecture. The key difference between the circuits is the 90° phase shifter structure producing the in-phase and quadrature carrier signals. Therefore, the operating frequency of the circuits is limited primarily by the bandwidth under which the phase accuracy of the phase shifters is acceptable and by the frequency limitations of the fairly standard BiCMOS processes, which also leads to excessive power consumption - for a minimum sized NPN $f_{max} = 8$ GHz at $I_E = 500 \mu\text{A}$ (paper I).

4.1.1 I/Q modulator with an analogue phase shifter

The modulator described in paper I was constructed in a 8 GHz 1.2 μm BiCMOS process (2.9 mm x 2.9 mm, ~ 50 mA from a 5.0 V supply) for a LO frequency range from 925 MHz to 960 MHz and a base band from 60 kHz to 500 kHz. It was shown that it is possible to implement an adjustable 90° phase shifter with adequate performance in the desired frequency range. The required LO suppression and image rejection of more than 35 dBc were reached under optimal operating conditions. However, both parameters were highly sensitive to operating conditions due to supply voltage and temperature dependent biasing, internal offsets and feedthrough.

A schematic diagram of the adjustable phase shifter used in the circuit is presented in Fig. 27. The circuit consists of two differential amplifiers with different emitter loads - capacitive or resistive. With the same input applied to both differential pairs, the phase difference between the outputs can be expressed as follows (Steyaert & Rooves 1992):

$$\phi = \arctan\left(\frac{2\pi f C_{\pi} r_{\pi} (R_S + r_b + R/2)}{R_S + r_b + r_{\pi} + (\beta + 1)R/2}\right) - \arctan\left(\frac{4C\pi f [(R_S + r_b + r_{\pi}) + C_{\pi} r_{\pi} / 2C]}{2 + g_m r_{\pi} - \omega^2 2C(R_S + r_b)C_{\pi} r_{\pi}}\right) - 90^{\circ}, \quad (20)$$

where β , g_m , r_{π} , r_b and C_{π} are the small signal parameters of the hybrid- π model of the transistors, R_S is the resistance of the source, and R and C are the emitter loads of the differential pairs. The frequency dependence of the phase in (20) is minimized when:

$$R \gg R_S + r_b \text{ and } C \ll (1 + \beta) / \omega^2 C_{\pi} r_{\pi} (R_S + r_b) \quad (21)$$

Furthermore, the gains of the differential pairs are equalized if:

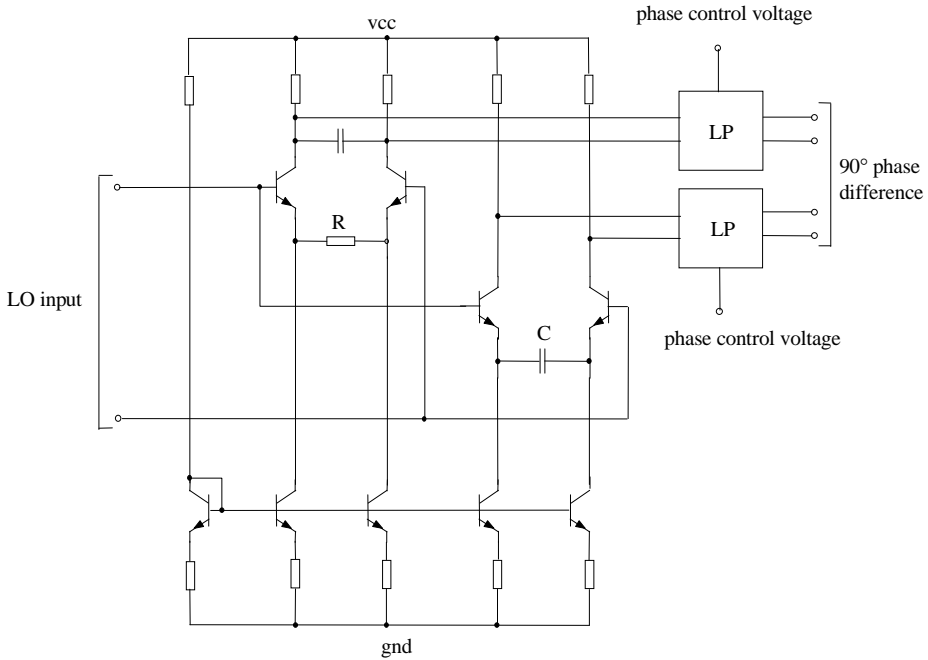
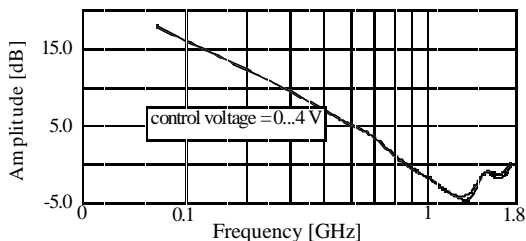
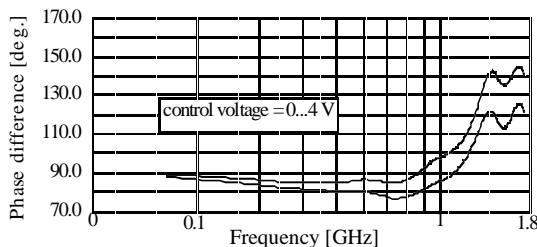


Fig. 27. Schematic diagram of the adjustable 90° phase shifter described in paper I.

Amplitude difference of the LO signals with extreme values of the control voltage



Phase difference of the LO signals with extreme values of the control voltage

**Fig. 28. Measured amplitude and phase differences of the 90° phase shifted LO signals.**

$$R = \frac{1}{2\pi f C} \quad (22)$$

The actual component values were first calculated using (20), (21) and (22), and the resulting values were later refined using circuit simulations. According to Monte Carlo simulations it soon became apparent that a sufficiently small phase error ($< \pm 2^\circ$) for 35 dBc image rejection could not be achieved without some form of phase trimming. Consequently, the phase difference is adjustable by two low-pass filters whose phase response can be altered by $\pm 5^\circ$. The phase adjustment is performed by varying the voltage over reverse-biased bipolar transistors, thus changing their transition capacitance and the overall time constants of the filters.

The measurement results of the phase shifter presented in Fig. 28. indicate that the amplitude difference between the in-phase and quadrature signals in the desired operating frequency range is about 2 dB, which does not pose any problems since the amplitudes are large enough to fully switch the currents in the Gilbert multipliers. The amplitude difference grows rapidly outside the desired operating frequency range due to the phase shifter topology. The lower graph in Fig. 28. demonstrates a phase error of less than 10° over a relatively large frequency range and an average 90° phase shift at the operating frequencies. The results given at the extreme values of phase control voltage show a phase adjustment range from 85° to 97° .

Under optimal conditions (i.e. $T = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, LO freq. 950 MHz 0.120 Vp-p, BB freq. 500 kHz 0.2 Vp-p) and with careful offset and phase trimming, the following results were measured: LO suppression $> 65\text{ dBc}$, Image rejection $> 65\text{ dBc}$, 3I suppression $> 46\text{ dBc}$, 5I suppression $> 57\text{ dBc}$. However, these results are highly optimistic due to careful pre-trimming not applicable in practice - in fact, if the circuit is

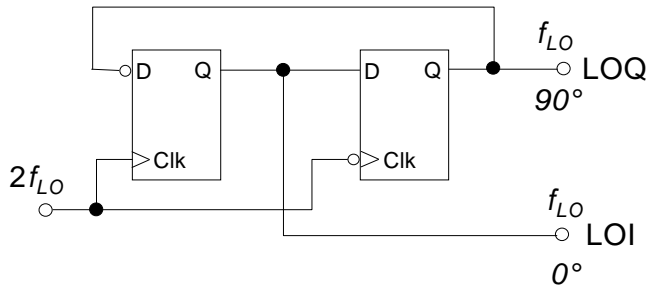


Fig. 29. Principle of the digital phase shifter.

left untrimmed, the LO suppression and image rejection degrade to roughly 30 dBc. Paper I provides a more detailed discussion on the output power, LO suppression, image rejection and harmonics behaviour of several samples of the modulator IC under different operating conditions.

4.1.2 I/Q modulator with a digital phase shifter

The modulator IC described in paper IV uses digital flip-flops to generate the internal in-phase and quadrature LO signals from an external signal having twice the frequency of the final carrier. The key advantages of the phase shifter topology shown in Fig. 29. is the wide operating frequency range and small sensitivity to process and operating condition variations owing to the symmetry of the structure – thus phase adjustment is not needed if offsets are minimized through careful design. The main disadvantage of the topology is the very high speed of operation required from the flip-flops – in this case $2f_{LO} \sim 2$ GHz. Furthermore, the $2f_{LO}$ signal must be highly symmetrical – i.e. 50% duty cycle – or non 90° phase difference will be produced. In order to minimize the effects of offsets in the phase shifter and multipliers related to the image rejection performance and LO suppression, respectively, common centroid structures and dummy devices were extensively used. A band gap reference was used for enhanced temperature stability. Because of the power hungry CML used to realize the phase shifter flip-flops, the circuit

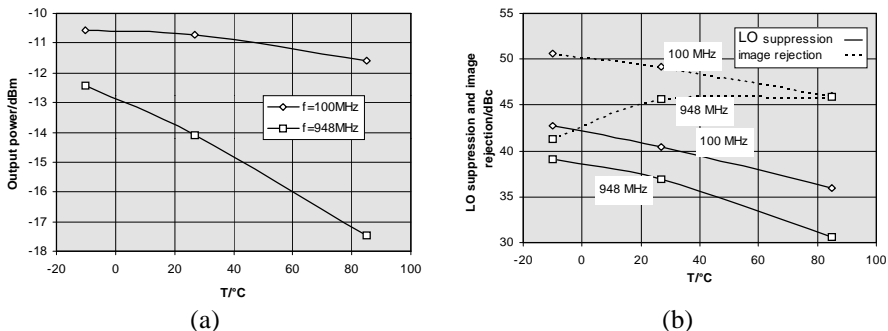


Fig. 30. Temperature behaviour of (a) output power and (b) LO suppression and image rejection at 100 MHz and 948 MHz ($V_{CC} = 5.0$ V).

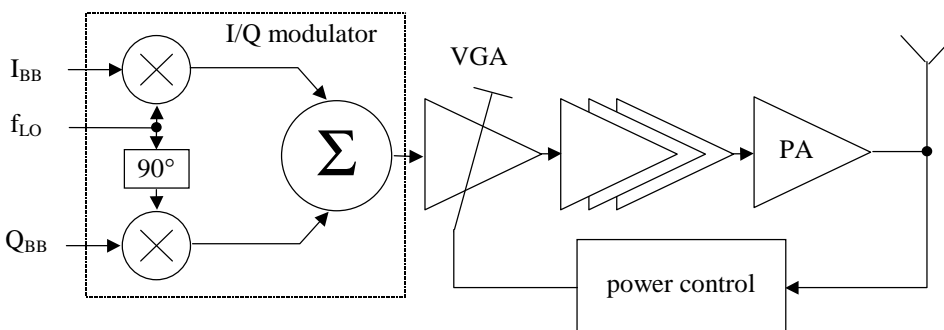


Fig. 31. Architecture of a sample base station transmitter.

uses more power than the previous modulator (~ 100 mA / 5 V supply), even though a faster $0.8 \mu\text{m}$ 12 GHz BiCMOS process was used. The circuit ($2.0 \text{ mm} \times 2.0 \text{ mm}$) was packed in a 28 pin SOIC for reduced feedthrough.

The measurement results of the fabricated chip are far superior to those measured of the modulator chip described in paper I – just about all specifications were met at all operating conditions. Depending on the frequency, the measured average output power is from -11 to -15 dBm, LO suppression is typically 38 dBc and image rejection 41 dBc. As shown in Fig. 30., temperature effects are small due to PTAT type biasing and careful layout design. However, performance degrades somewhat at frequencies over 800 MHz possibly due to the band limiting effects of packaging parasitics and output capacitances of the open collector type output. A $\pm 1.0^\circ$ accuracy of the internal phase shifter was calculated from the measured image rejection.

4.2 Variable gain amplifiers

The purpose of this study was to investigate the level of performance achievable with an integrated variable gain amplifier (VGA) in the 1 GHz frequency range using a fairly standard BiCMOS process. RF amplifiers with controllable gain are used in many applications either as a separate block or as part of an automatic gain control system. For example, in a modern radio telecommunications system VGAs are used to keep signal levels constant regardless of distances or some unpredictable changes in the channel between the base station and the mobile unit.

The amplifiers discussed in papers III and VI were designed for an existing transmitter architecture in a GSM base station shown in Fig. 31. usually made of discrete component or hybrid circuits. The BiCMOS process was used, because other high-frequency parts of the system use BJTs, thus enabling future integration of a larger part of the system – e.g. combining the VGA circuit and the preceding I/Q modulator. The pre-design specifications were: max. 10 dB power gain, over 1 GHz bandwidth, voltage-voltage linear gain control with 47 dB dynamic range, output noise density less than $23 \text{ nV}/\sqrt{\text{Hz}}$,

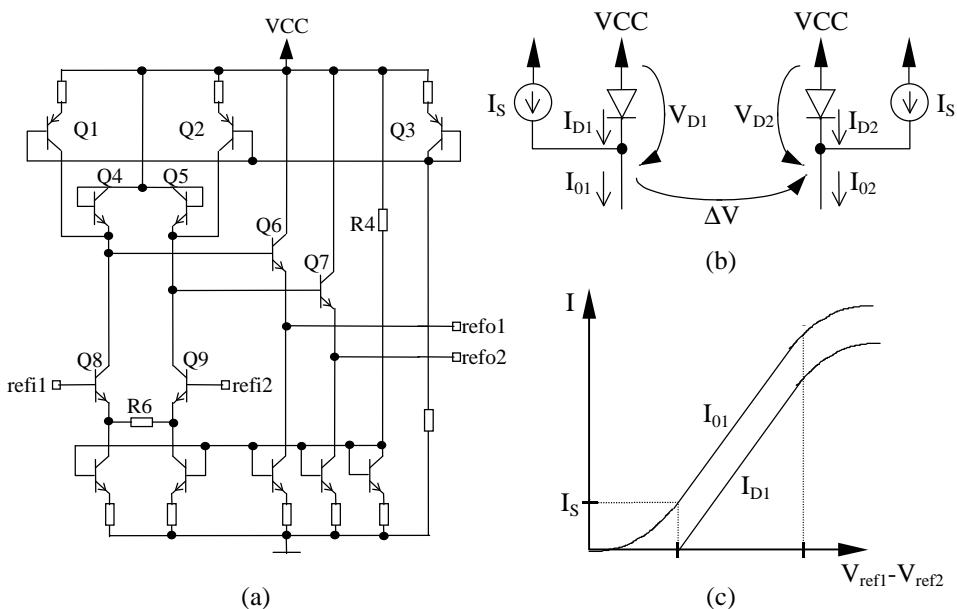


Fig. 32. The gain control linearization circuitry. (a) The schematic diagram, (b) the principle of operation and (c) the diode current.

-1 dB output compression power exceeding -2 dBm and gain control bandwidth more than 10 MHz.

4.2.1 The basic variable gain amplifier

The first variable gain amplifier described in paper VI was implemented in a standard 8 GHz 1.2 μm BiCMOS process. A Cherry-Hopper type gain stage (Cherry & Hopper 1963) was used to provide most of the available gain and a Gilbert type variable gain cell was used for gain control. The output voltage of the variable gain cell can be expressed as (see Fig 3. (b) in paper VI):

$$V_o = R_C(I_{c1} - I_{c4}) = \frac{R_C(I_{c5} - I_{c6})}{1 + e^{-\frac{V_{agc}}{V_T}}}. \quad (23)$$

Since the gain ($\propto V_o$) of the variable gain stage varies exponentially when a linear control signal is employed, some kind of pre-processing of V_{agc} was needed to produce a linear dependency between the gain and the control voltage. The preprocessing circuitry is formed of a degenerated differential pair shown in Fig. 32. (a) (Q8 and Q9), the output of which is connected through a pair of diode connected transistors (Q4 and Q5). The effect of the base currents of the AGC stage quad on the diode currents is reduced by emitter

followers (Q6 and Q7). PNP transistors Q1 and Q2 act as current sources, which help to linearize the diode currents, as will be explained shortly. The diode current is shown graphically in Fig. 32. (c) with references to Fig. 32. (b). In order to have a linear dependency between the controlling signal and the gain, the voltage signal ΔV driving the agc circuit should be of the form:

$$\Delta V = V_{D1} - V_{D2} = V_T \ln \left(\frac{I_{D1}}{I_{D2}} \right), \quad (24)$$

where $V_T = kT/q \approx 25$ mV, I_{D1} and I_{D2} are the diode currents. Now, if the quad is driven with voltage ΔV , one can write the following formula for the output voltage of the agc block (23) (infinite β assumed)(Meyer & Mack 1991):

$$V_o = \frac{R_C(I_{C5} - I_{C6})}{1 + e^{(-\Delta V)/V_T}} = \frac{R_C(I_{C5} - I_{C6})}{1 + e^{-V_T \ln \left(\frac{I_{D1}}{I_{D2}} \right) / V_T}} = \frac{R_C(I_{C5} - I_{C6})I_{D1}}{I_0}, \quad (25)$$

where $I_0 = I_{D1} + I_{D2}$. As equation (25) shows, V_o and the gain, for that matter, is a linear function of I_{D1} . Thus, the problem of linearizing the gain control reduces down to forming a circuit to produce as linear current signals I_{D1} and I_{D2} as possible. The obvious way to do this is to use the output current of a differential pair, since currents I_{D1} and I_{D2} are essentially differential. However, the output current of a simple differential pair is a linear function of the input voltage only over a limited range determined by the emitter current and emitter resistance (Gray & Meyer 1983). This poses a problem since at high attenuation one of the diode currents must go to zero, which resembles the most non-linear section of the output current curve of the differential pair. This problem is overcome by the current sources connected parallel to the diodes as shown in Fig. 32. (b). Now, if, for example, I_{O1} equals I_s the current through the resembling diode is ideally zero – see Fig. 32. (c). Thus, if I_s is large enough, the diode current can, in theory, be made zero before I_{O1} becomes non-linear. However, in practice the saturation of the PNP transistors makes the operation of the circuit somewhat more complex, especially at extremely low diode currents. The linearity of the control was further enhanced by using transient simulation for tuning the ratio between emitter areas of the quad and diode connected transistors. Thus, capacitive effects were taken into account in the final simulations. The difference between the gain vs. control voltage predicted by DC and transient simulations after the linearity was optimized using transient analysis is depicted

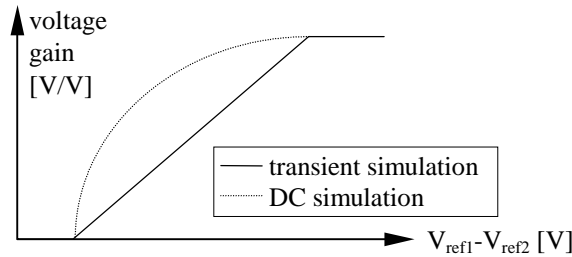


Fig. 33. Gain vs. control voltage characteristics predicted by transient and DC simulations after the linearity was optimized using transient analysis.

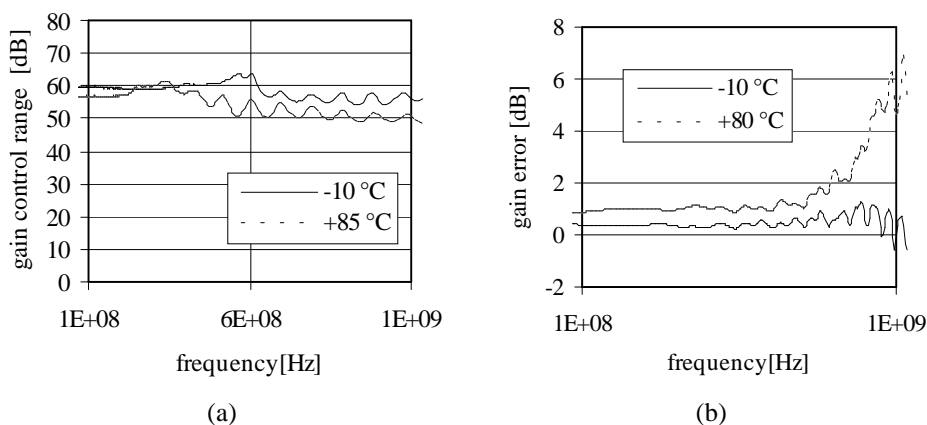


Fig. 34. (a) Gain control range and (b) gain error from the max. gain at $T = 21\text{ }^{\circ}\text{C}$ at extreme temperatures.

in Fig. 33. Transient simulation was also used to check the bandwidth of the gain control.

The maximum differential gain of the circuit ($1.15 \times 2.15\text{ mm}^2$, 40 mA, 5 V) is 10 dB with over 1 GHz bandwidth and -6.9 dBm input -1 dB compression power. Gain adjustment range of 50 dB at 200 MHz and 38 dB at 960 MHz were measured with single-ended input. With differential input the control range is > 50 dB also at 1 GHz, which is quite large when compared with similar circuits reported by Hauptmann et al. (1992), Reimann & Rein (1989), Meyer & Mack (1991) and Sansen & Meyer (1974), for example. Other measurement results at the nominal operating conditions ($T = 22\text{ }^{\circ}\text{C}$ and $V_{CC} = 5.0\text{ V}$) are:

- The input referred -1 dB output compression power: -8.1 to -6.6 dBm depending on the frequency.
- TOI (Third Order Intercept) point is -0.48 dBm.
- The output noise is from 18.8 to $24.8\text{ nV}/\sqrt{\text{Hz}}$ depending on the gain.
- The -3 dB bandwidth of the gain control is more than 10 MHz.

The main problems with the circuit was the sensitivity of gain to temperature and supply voltage variations and the level of noise, which were the main reasons for the design of the VGA circuit described in the next section (paper III).

4.2.2 Temperature stabilized variable gain amplifier

The VGA chip described in paper III enhances the noise and gain control range of the previous amplifier. The gain of the first stage was increased and PTAT and band gap type references were used to stabilize the gain against changes in operating conditions. Because of its simpler biasing, a cascaded gain stage was used instead Cherry-Hopper

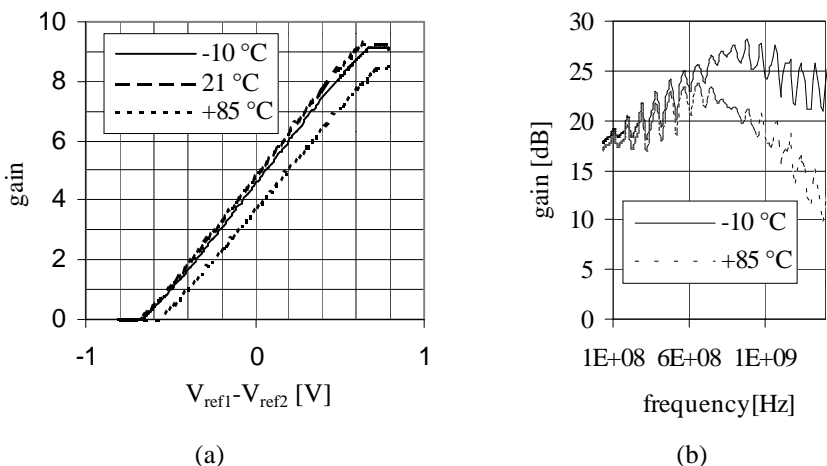


Fig. 35. (a) Gain vs. control voltage at different temperatures ($V_{CC} = 5.0$ V and $f = 100$ MHz) and (b) reduction of gain peaking at higher temperatures.

topology to provide most of the gain. As shown in Fig. 34. (a), the gain control range, with differential input, is > 50 dB at almost all frequencies and temperatures, and in Fig. 34. (b) the maximum measured differential gain (~ 18 dB at 100 MHz) at $T = 21$ °C varies less than 1 dB at frequencies below 800 MHz and temperatures from -10 °C to 85 °C – most of the error happens at high temperatures as also seen in Fig. 35. (a). The gain peaks at high frequencies, thus, the maximum gain of 25 dB is reached around 1 GHz at -10 °C. The peak is highly sensitive to temperature, as shown in Fig. 35. (b), which leads to 6 dB lower gain at $T = +85$ °C ($f = 1$ GHz). This phenomenon is believed to be caused mainly by the resonance between the package parasitics and the collector capacitances of the open collector outputs, which grow larger at high temperatures due to PTAT type biasing. The noise spectral density at the output is typically -135 dBm/Hz (~ 40 nV/ $\sqrt{\text{Hz}}$, the increase in the noise compared to the previous VGA is due to the added gain) at 950 MHz and TOI is 15 dBm at 100 MHz dropping to 8 dBm at 950 MHz. The chip, which is extremely insensitive to supply voltage variations, consumes about 100 mA from a 5.0 V supply and uses 1.15×2.00 mm² of silicon.

4.3 Frequency synthesis circuits

Papers VII through X describe three circuits for RF and IF frequency synthesis, all with the same basic structure shown in Fig. 36. (paper IX), which includes an RF input amplifier for the VCO signal, a dual or multi-modulus divider, CMOS counters for the reference and VCO signal and a phase frequency detector with programmable or fixed voltage or current output. Additionally, the synthesizer described in paper IX contains structures for automated speed-up of frequency hopping, which includes switching of the phase detector gain and loop filter elements. The maximum output frequency in all cases

is in the neighbourhood of 2 GHz, while the maximum external reference frequency varies from 20 MHz (papers VII and VIII) up to 200 MHz (paper IX).

The frequency synthesizer chips described here act as integer-N type synthesizers. The VCO input is first converted to CML-level signals, which drive the CML dual modulus prescaler. The prescaler modulus is selected appropriately to keep the output frequency of the prescaler almost constant at VCO frequencies fit for the GSM (~1 GHz) and the DCS (~2 GHz) system. A programmable M counter and pulse swallow (PS) counter are used to control the ratio between division by n or $n+1$ by the prescaler. Therefore, the final output frequency of the divider and DMD combination can be expressed mathematically as:

$$f_{ref} = \frac{f_{VCO}}{nM + A}, \quad (26)$$

where f_{ref} is the reference frequency, f_{VCO} is the input frequency (VCO output freq.), n the division ratio of the $n/n+1$ dual-modulus prescaler, M is the division ratio of the M counter and A is the division ratio of the pulse swallow counter.

The reference signal is a CMOS level signal, which is applied after (optional) division to the internal PFD. The voltage pulses at the output of the PFD are converted to current pulses (papers VIII and IX) by the programmable current pumps. The programmability facilitates the use of the circuit in existing applications. However, it is also used to boost the pull-in ability in frequency hopping applications. All internal registers are programmed with serial (papers VIII and IX) or parallel (paper VII) data depending on the number of pins available in the circuit package and lack of BJTs in the case of the semi-custom circuit.

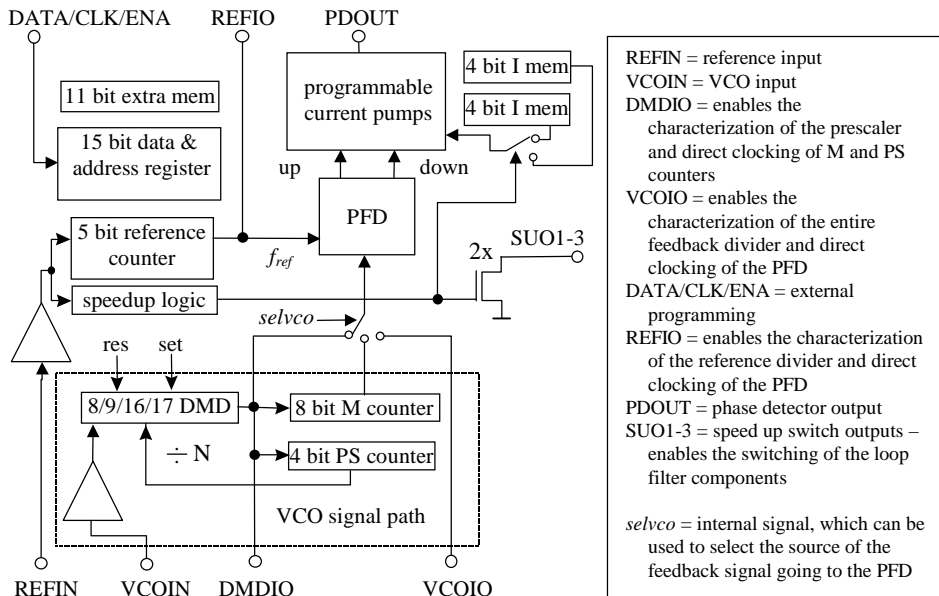


Fig. 36. Architecture of the synthesizer described in paper IX.

The synthesizer described in paper IX acted as the starting point for a synthesizer study. An integer-N based PLL synthesizer was selected as the basis for the design because of its simple structure and suitability for various applications in radio base station architectures. The design specifications, such as the length of counters and the ranges of VCO and reference frequencies were loosely derived from various existing GSM base station applications which soon led to the decision to leave the VCO and the loop filter out of the IC for enhanced flexibility – for a versatile PLL chip, it makes sense to leave the selection of the VCO and the loop filter to the loop designer rather than to the IC designer whereas for a fixed application, with a set frequency range and loop properties, the integration of the VCO and the loop filter should probably be reconsidered.

Various loops working in the region of 1 GHz and incorporating the PLL IC were designed and measured. All test boards used a second order current driven passive integrator as the loop filter with extra filtering of the reference spurs (i.e. notch at the 1st reference frequency harmonic and post-filtering of the higher order reference harmonics). The main specifications of the loops with f_{ref} of 10 MHz or 20 MHz were a frequency settling time of less than 10 μ s and over 45° phase margin in the closed loop frequency response. These specifications were derived from the system level specifications of an actual future transmitter architecture being developed for a GSM base station, and the purpose of the synthesizers developed here were to produce rough, non-200 kHz frequency steps very fast.

The output phase noise of one of the above-mentioned loops at 100 kHz offset is shown in Fig. 37. The level of noise depends on the current level of the PFD output, the raise of which increases the output noise of the PFD while the output level of the VCO stays the same. The behaviour of the reference harmonics as a function of the PFD output current is shown in Fig. 38. This figure clearly shows the increase in the level of the harmonics with the increase in the level of the PFD output current. As expected, the level of the 1st harmonic is reduced considerably by the notch in the frequency response of the loop filter. According to the measurements, the levels of the reference harmonics are not strong functions of the temperature. However, this might not be true, if the notch in the loop filter response is temperature dependent.

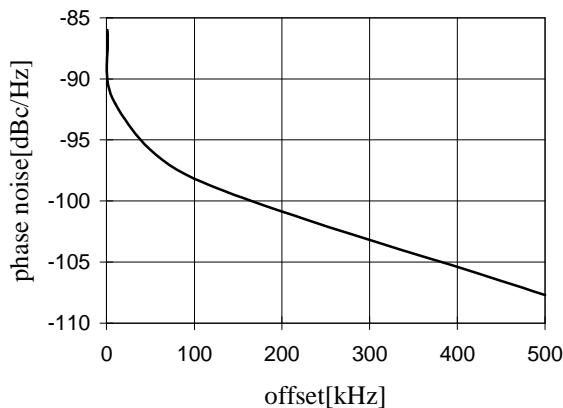


Fig. 37. Phase noise of an example synthesizer.

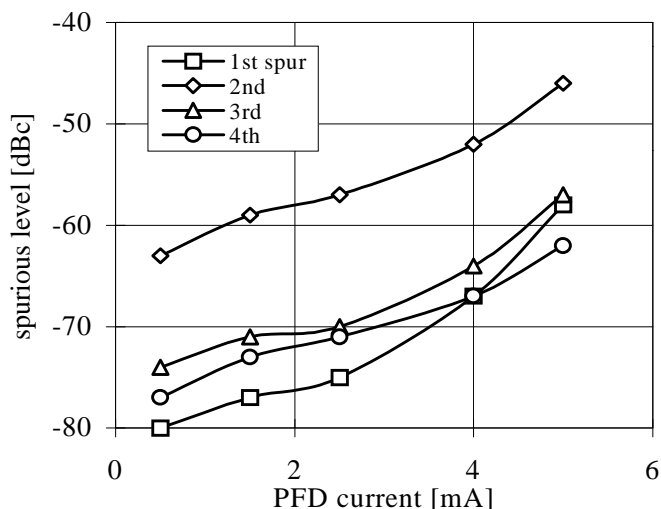


Fig. 38. Behaviour of the reference spurious signal.

The frequency step response of the synthesizer is shown in Fig. 39 as a function of temperature (a) ($I_{\text{PFD}} = 5.0 \text{ mA}$) and as a function of the PFD output current ($T = +27 \text{ }^\circ\text{C}$)(b). The magnitude of the step was 20 MHz in all measurements and the voltage waveform at the output of the loop filter was used to represent the response. As can be seen in Fig. 39. (a), the settling time is quite independent of temperature as expected, since a band gap reference was used to generate the PFD output currents. The change in the loop dynamics caused by the change in the phase detector gain constant (K_D) as a function of the PFD current programming is readily demonstrated in Fig. 39. (b). Thus, the smaller the programmed PFD output current, the more unstable the response. Even with maximum current the required 10 μm settling is not achieved. This is mainly due to the uncertainties in the loop design parameters, such as the VCO gain factor (K_V), input capacitance and modulation bandwidth, as well as the PCB parasitics.

During the period of time when the first synthesizer was being designed, an opportunity to test the suitability of a bipolar semicustom process for a similar application came up (paper VII). The process in question was a bipolar transistor array with strategically placed passive components meant for rapid prototyping of telecommunication circuits. The main features of the process were:

- NPN $f_T = 27 \text{ GHz}$.
- Minimum emitter area = $0.8 \times 1.6 \text{ } \mu\text{m}^2$.
- Minimum transistor area = $5.4 \times 8.1 \text{ } \mu\text{m}^2$.
- Poly resistors up to $600 \text{ } \Omega/\square$.
- 3 layers of gold interconnect.
- Trimmable microme resistors ($50 \text{ } \Omega/\square$, $\text{TCR} < 200 \text{ ppm}/^\circ\text{C}$).
- Schotky diodes and lateral PNPs.
- Deep trench isolation.
- Internal ESD structures.

The available components are summarized in Table 6. It soon became obvious that there were not enough active components in the transistor array to duplicate the earlier BiCMOS design in full. A careful analysis was carried out to predict the number of components used for different synthesizer architectures derived from the earlier design. The analysis consisted of a design of basic circuit structures such as CML flip-flops and stacked logic using the preset selection of active and passive components. Using the component counts of these basic building blocks, a prediction of the total component consumption was calculated with a spreadsheet program. According to the analysis made, some of the circuit structures were left out or simplified. The reference divider was left out altogether, the size of the pulse-swallow counter was minimized, and the digital current programming was left out, because no appropriate PNP transistors were available for the sourcing charge pump. Only sinking sources were used and the programming of the counters was changed from serial to parallel. Because a major part of the active components was consumed by the main counter, a series of two-bit Johnson counters were used to realize the 10 bits needed.

The biggest surprise during the design of the semicustom circuit was the amount of time it took to complete the design – semicustom technology is primarily meant for rapid evaluation of electrical circuits and systems. However, the speed advantage of the semicustom technology when compared to a full custom one is in the speed of processing rather than in the speed of design. Actually, when integrating a large system, some extra time must be spent on evaluating the amount of circuit functions one can fit into a preset array of transistors. Additionally, when the design contains a large number of similar circuit structures, flip-flops, logic ports etc., the time spent preparing the layout is much smaller in a full-custom environment, because repetitive copies of the interconnects cannot in most cases be used in a semicustom design. This leads to a very time consuming routing job even with three levels of interconnects.

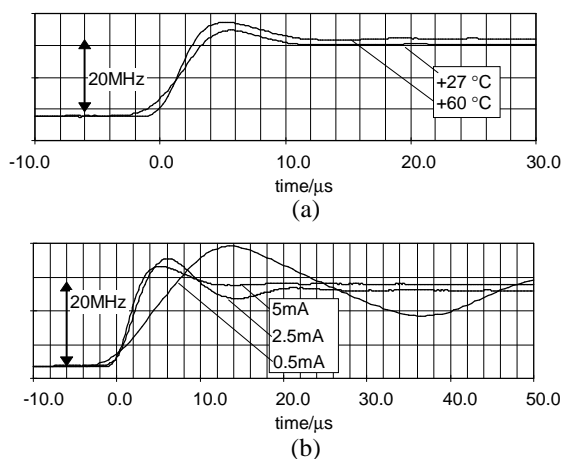


Fig. 39. (a) Frequency step response at $T = -10$ and $+60\text{ }^{\circ}\text{C}$ (IPDF = 5.0 mA) and (b) at various PFD currents ($T = +27\text{ }^{\circ}\text{C}$).

Table 6. Components available in the QC9-60D array.

component	no.	comment
NPN	1022	different sizes
lateral PNP	176	different sizes
diodes	426	
capacitors	158	116 pF total
polyresistors	2008	6 822 400 Ω total
supply and ESD protection structures		
isolated substrate areas		

The experience accumulated during the design and measurements of the earlier synthesizer circuits were exploited in the design described in paper IX, where a more application specific synthesizer circuit is discussed. However, the circuit is still meant for both IF and RF synthesis, but the selection of division ratios of the feedback divider and the reference divider were known before the design began. This led to the design of a new multi-mode prescaler as described in paper IX. Also, the maximum external reference frequency was increased to 200 MHz and maximum operating frequency of the phase detector to 80 MHz for added flexibility. Minimization of the phase-noise of the phase detector was one of the main design goals. This led to a new programmable charge pump topology based on the op-amp current mirror. Due to the noise properties of the previous phase-frequency detector, a new dual-mode phase frequency detector was designed. A two-fold speed-up logic as shown in Fig. 40. was added for frequency hopping applications. First, the level of the current pulses of the PFD is automatically changed to an alternate preprogrammed value for the duration of the speed-up. Second, a pair of MOS switches can be used to dynamically change the time constants of the loop filter during frequency transition. The various new circuit structures are described in paper IX. A more detailed discussion of the design and properties of the new low-noise charge pump topology shown in Fig. 41. based on the op-amp current mirror (Hosticka 1979, Bult & Geelen 1990) is presented in paper X. The most significant points discussed

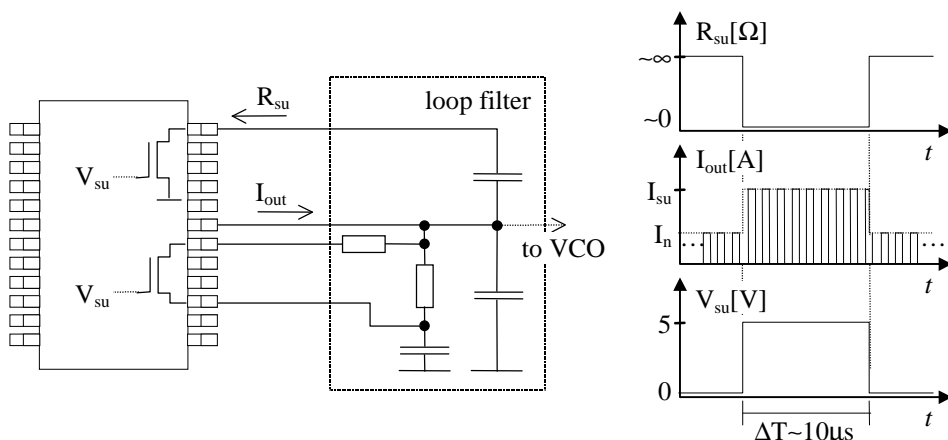


Fig. 40. Principle of the speed-up logic. PFD gain constant (KD) switching and loop filter time constant switching.

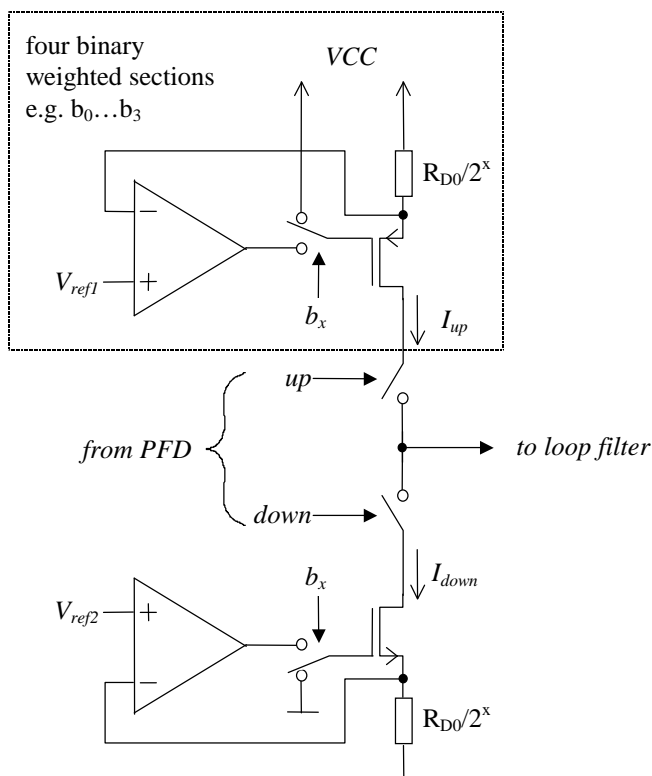


Fig. 41. Principle of the low-noise charge pump.

in this paper include the design of op-amp based current mirrors and their use in a digital-to-current converter with low noise, a large output voltage range and an excellent current balance. From the noise point of view, the main benefit of the structure presented is the reduction of the $1/f$ noise of the active device below that of the current setting source resistor at a very low frequency (Fleischer 1989). At the same time, feedback forces the output current to V_{ref}/R_S , which effectively increases the output resistance of the source approximately to (Johns & Martin 1997)

$$R_{out} \approx g_m r_{ds} R_S (1 + A), \quad (27)$$

where R_S is the resistance of the source-to-ground resistor, A is the absolute value of the op-amp's gain, g_m is the small-signal transconductance and r_{ds} the drain-to-source resistance of the active device. Due to the increase in the output resistance, the output current is almost independent of the properties of the transistor as long as the op-amp gain is sufficient. The approximate noise density of the output current was derived, and it can be presented as

$$S_{out} = S_{in1} \left[\frac{R_{ref}}{R_S} \right]^2 + S_{in2} + S_{vn1} \left[\frac{1}{R_S} \right]^2 + \frac{2kT}{R_S}, \quad (28)$$

where R_{ref} is the output resistance of the reference voltage source, S_{vn1} is the voltage noise density of the op-amp's input referenced voltage noise source, k is Boltzmann's constant, T is absolute temperature and S_{in1} and S_{in2} are the current noise densities of the op-amp's input referenced current noise sources.

The output noise of a 4-bit programmable current source can now be presented as

$$\sqrt{S_{tot}} = \sqrt{\sum_{i=0}^3 (S_{out})_i \cdot b_i}, \text{ where} \quad (29)$$

$(S_{out})_i$ equals the output current noise density of a one bit digital-to-current converter section (I_D of sections 0 through 3 are 0.5, 1.0, 2.0 and 4.0 mA, respectively) and b_i is the value of the i^{th} bit of the 4-bit code word. As a result of the formulation, it was pointed out that in order to design a digital-to-current converter with the required $-155 \text{ dBc}/\sqrt{\text{Hz}}$ noise level, one only needs to design the section with the lowest output current to meet that noise specification and then scale the section for a higher output current.

Another interesting technique shown in Fig. 42. is the use of a voltage follower to minimize some of the transient effects generated during switching, which degrade the

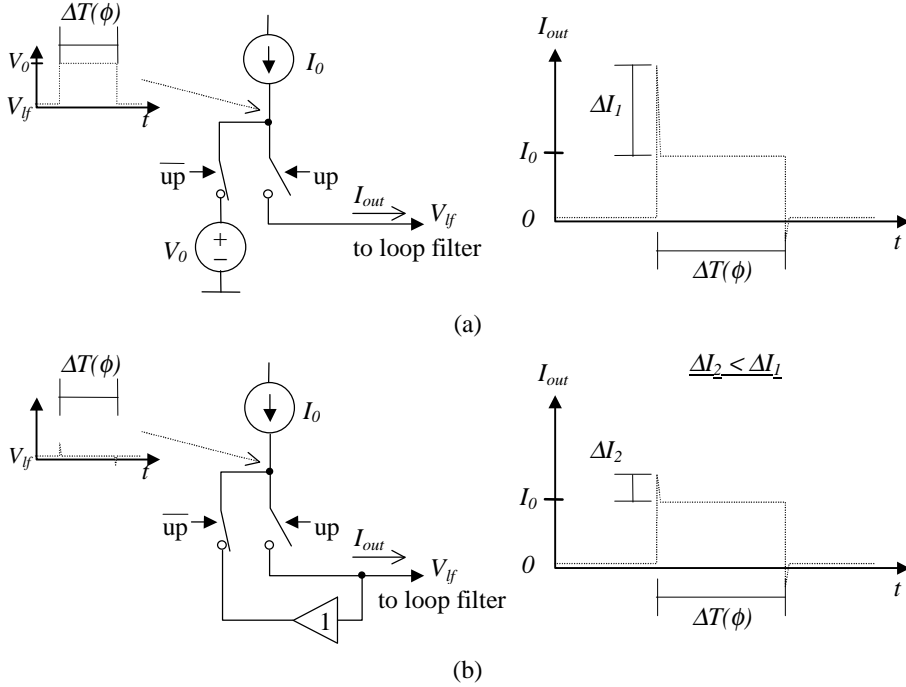


Fig. 42. Principle of transient cancellation. Output current pulse without (a) and with (b) feedback.

purity of the final synthesized signal (Rhee 1999). The enhancement is achieved by keeping the voltage over the digital-to-current converters constant between their on and off states.

The measurements indicate that the output voltage range of the charge pump extends from 0.7V to 4.3V, the current error for output currents below 7.5 mA is less than 3%, the output resistance is around 10 M Ω and the output current noise density is 18.7 pA/ $\sqrt{\text{Hz}}$ at 5 kHz for an output current of 500 μA . It was found out during design and measurements that for maximum benefit the minimization of the input referred voltage noise of the op-amp and the supply noise sensitivity of the complete charge pump structure must be taken into account.

During loop measurements of the complete PLL the level of the 1st reference spur without notch in the loop filter at 10 MHz offset was -62.4 dBc, with closed loop bandwidth of 300 kHz, $f_{\text{ref}} = 10$ MHz, $f_{\text{out}} = 930$ MHz and $I_{\text{PD}} = 3.5$ mA (i.e. the current word is 7). Higher order reference spurs could not be detected during measurements. The level of the 1st spurious signal is thus some -14 dB better than that of the 1st PLL circuit (in Fig. 38. the 2nd spurious signal ≈ -54 dBc, thus the level of the 1st spurious without notch in the loop filter is -48 dBc, if 20 dB/dec attenuation outside the loop bandwidth is assumed). This enhancement is due to the better current balance provided by the op-amp charge pump. However, the measured 3% error in the current balance should theoretically (equations (15) and (17)) give -75 dBc spurious at the reference frequency. The degradation in performance is most likely due to the poorer charge balance at 10 MHz than predicted by the DC measurements. Of course, the current balance is not the only source of reference spurs as described in the preceding chapter.

One way to find out how much the noise properties of the synthesizer were affected by the new charge pump circuitry is to compare the synthesizers described in papers VII and IX using the concept of 1 Hz normalized phase detector noise floor defined in Banerjee (1998), for example:

$$PN_{1\text{Hz}} = PN - 10\log(f_{\text{ref}}) - 20\log(N), \quad (30)$$

where PN is the measured phase noise, f_{ref} is the reference frequency and N is the feedback division ratio. Equation (30) allows comparison of the phase noise performance of synthesizers which use different reference frequencies and feedback ratios. According to the measurements, the 1 Hz normalized phase detector noise floor of the synthesizer with the new charge pump circuitry is 3 dB better (i.e. -210 dBc/Hz).

The operation of the speed-up was tested using a similar configuration to that used in the National's Fast Lock system (National SemiconductorTM 1997) and shown in Fig. 43. (a). The basic benefit of this simple system is that only a resistor is switched, thus no precharging of capacitors is needed to avoid glitches at the end of the speed-up. In the following discussion the results for a 7.65 MHz frequency hop to within $tol = 100$ kHz from the final output frequency are discussed. Reference frequency $f_{\text{ref}} = 7.65$ MHz, output frequency $f_{\text{out}} = 810$ MHz, phase detector gain $K_D = 0.2$ mA/rad, VCO gain $K_V = 8$ MHz/V, $R_2 = 1540 \Omega$, $C_2 = 22$ nF and $C_3 = 2.2$ nF were used, because the same loop will be used in the next chapter, when a new speed-up scheme based on the direct control of the loop filter charge is introduced.

During measurements the output current level of the PFD was switched four times higher during channel switching than during the normal, low noise/low spur signal, operation. The main purpose of the increased current level and thus the increased phase detector gain is to increase the bandwidth of the loop, thus making the frequency transition faster. However, as the increased phase detector gain makes the loop bandwidth wider, it also increases the damping factor of the loop, which has a counter-productive effect on the settling time. Mathematically this effect can be seen by considering equation (12), which gives the approximate lock time of the loop and the equations for the natural frequency ω_n and the damping factor ζ of a charge pump PLL (Larsson 1995):

$$\omega_n = \sqrt{\frac{K_D K_V}{NC_2}} \quad (31)$$

$$\zeta = \omega_n R_2 C_2 / 2, \quad (32)$$

where K_D = phase detector gain = $I_{PD}/2\pi$, K_V = VCO gain and R_2 and C_2 are the resistance and capacitance of the loop filter components shown in Fig. 43. (a). Clearly, if the phase detector output current I_{PD} is increased, both the natural frequency and the damping factor increase. Therefore, as one considers equation (12), it seems at first that increased ω_n and ζ shorten the lock time because they both appear in the denominator. However, the damping factor also appears in the nominator and has a strong counter effect on the lock time especially when approaching unity. This effect can be readily seen in Fig. 43. (b), where the lock time L_T vs. PD output current I_{PD} is plotted. The behaviour of L_T in the 1st case, where only the PD output current is increased, is presented as the curve labelled R_2 . As shown, only a minor improvement in lock time may be achieved, because the increasing damping factor will make the lock time increase for PD output currents near and above 1 mA.

The problem caused by the increased damping factor is cancelled out when the value of the loop filter resistor R_2 is changed during the speed-up to keep the damping factor

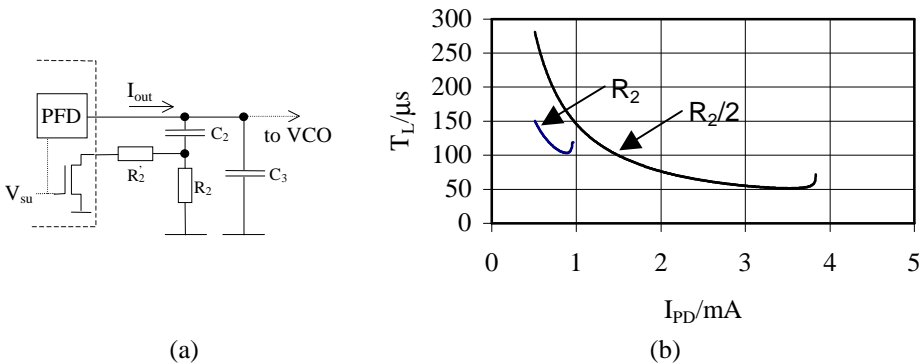


Fig. 43. (a) Speed-up configuration used during measurements and (b) behaviour of lock time as a function of the PFD output current with and without resistor switching.

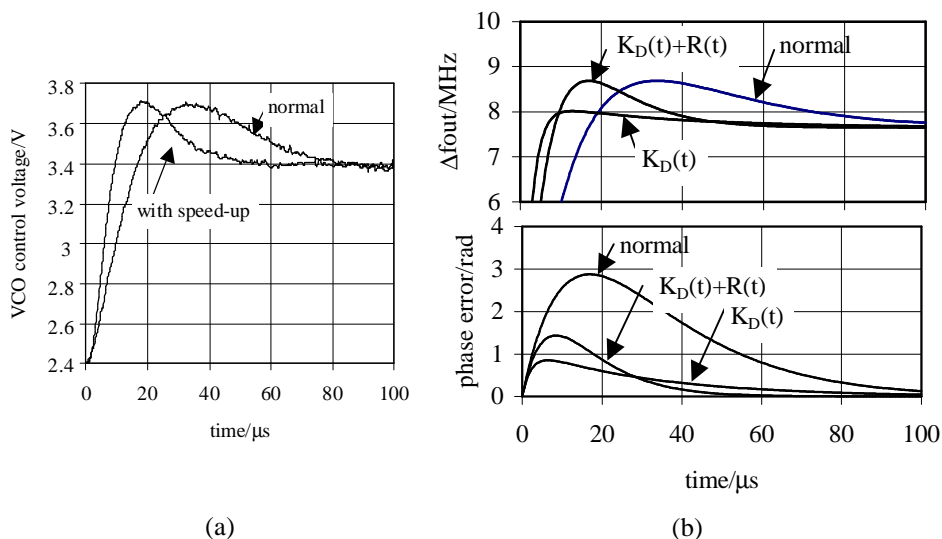


Fig. 44. (a) Measured frequency step response of the loop with and without speed-up and (b) simulated output frequency and phase error.

constant. This is accomplished by connecting the second resistor R_2' in Fig. 43. (a) in parallel with R_2 , thus lowering the effective resistance for the duration of the speed-up period. In our case the two resistors have the same value, thus the parallel connection will have one half of the original resistance R_2 . As mentioned above, the PD gain K_D was four times higher during the speed-up period, which produces twice the original natural frequency ω_n as given by equation (31). Thus, when one considers equation (32), halving the value of the original R_2 will keep the damping factor constant. The behaviour of the lock time as a function of the PD output current in this 2nd case is labelled $R_2/2$ in Fig. 43. (b). As can be seen, the minimum lock time is now around 50 μs compared to 100 μs of the case where the resistor was kept constant.

The measured frequency step responses of a normal loop and a loop with the speed-up described above are shown in Fig. 44. (a). Corresponding mathematical results of a 2nd order loop are shown in Fig. 44. (b). Clearly, the measurements and simulations match well. To illustrate further the benefit gained by the resistor switching, the frequency and phase responses for the case where the resistor stays constant, are also plotted in Fig. 44. (b) (labelled $K_D(t)$) contrary to the case where the resistor is switched, which is labelled $K_D(t)+R(t)$). From the phase error curves, it can be seen that the maximum phase error is smaller, when the resistor is kept constant. However, the decay of the phase error towards zero is much slower than in the case where the resistor value is halved during speed-up. According to the mathematical model, the time it takes in each case to reach phase error below 6 deg. is 45 μs , 67 μs and 105 μs , respectively. Based on these values, it was found out that simply using the speed-up method just described, it would not be possible to simultaneously achieve adequate frequency step speed and low level of reference spurs for future applications. Therefore in the next section a new speed-up method will be proposed, which further speeds-up the frequency step response of an integer-N PLL.

5 Speeding up an Integer-N PLL by Controlling the Loop Filter Charge

5.1 Introduction

When used in modern telecommunications systems, one of the problems associated with integer-N phase-locked loop based synthesizers is the unacceptable level of spurious signals at the frequencies of the adjacent channels when the loop bandwidth is large enough to allow fast channel switching. Papers XI and XII study a group of methods based on current signals connected to the loop filter designed to speed up the frequency step response of integer-N PLLs, thus allowing the increased speed to be later traded off to lower output spurious signals by lowering the closed loop bandwidth of the loop. First the optimal speed-up waveforms are found mathematically using a linear PLL model. Paper XII also discusses problems associated with this theoretical waveform and introduces a considerably simpler waveform based on the use of two current pulses. This method uses excess output frequency to quickly cancel the accumulated phase error. In order to accelerate the decay of the phase error, the PLL is first overdriven at the beginning of the frequency transition with an external charge pulse to the loop filter. As the phase error goes rapidly to zero, the frequency error is also reduced to zero by another charge pulse. The presented theory is verified by measurements using a practical RF synthesizer.

5.2 Overview of the methods

In the methods studied henceforth, the voltage at the input of the VCO is changed to a new, desired, value with the aid of an out-of-the-loop circuitry controlling the charge stored in the loop filter. This so-called speed-up circuitry is only connected to the loop for

a short period of time during the interval within which the synthesizer changes its frequency. Thus, during normal operation, the extra circuitry does not disturb the operation of the loop by adding noise or modifying the loop filter transfer function, for example. Additionally, since the speed-up structures are contained in a completely separate piece of circuitry, they do not require any - possibly performance degrading - changes to be made to the existing loop components, such as the VCO, phase detector and dividers. The additional circuitry is also well suited for integration - one of the starting points of the study - since it only consists of programmable current and/or voltage sources.

The concepts of the four speed-up methods considered in paper XII are shown in Fig. 45. The charge stored in the loop filter is controlled by the current and voltage sources - the two principal methods for delivering a predetermined amount of charge to capacitors C_2 and C_3 - shown in Fig. 45. (a) through (d). The first two methods use additional current signals to set the state of the loop filter. In Fig. 45. (a), a single current source I_1 is connected directly to the loop filter. In Fig. 45. (b), each capacitor has an additional

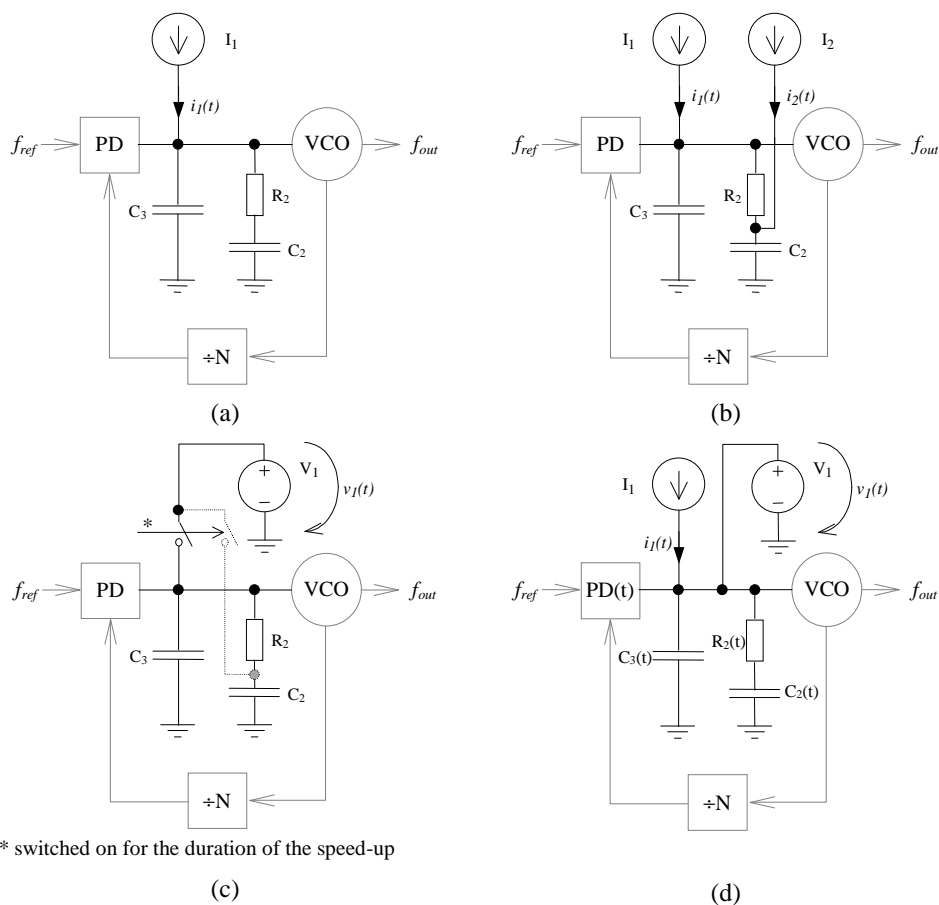


Fig. 45. Alternate speed-up configurations. (a) shared source (b) dedicated source (c) voltage driven and (d) hybrid methods.

current source I_1 and I_2 , thus allowing more controlled charging. In the circuit shown in Fig. 45. (c), the loop filter is forced to the desired voltage by an additional voltage source V_1 . Finally, Fig. 45. (d) depicts a circuit based on a mix of the first two speed-up schemes with an additional current source I_1 and an additional voltage source V_1 . For improved generalisability, the phase detector gain $K_D(t)$ and the values of the loop components $C_2(t)$, $C_3(t)$ and $R_2(t)$ are marked as time dependent. Thus, their values can also be controlled during frequency hops.

The following chapters aim at finding optimal $i_1(t)$ and $i_2(t)$ waveforms which minimize the phase and frequency error at the end of the frequency hop period. Fig. 46. shows an example of the behaviour of the output frequency and output phase error. Here, the output frequency f_o changes from f_0 to f_1 during the frequency hop initiated at $t = 0$ s. Now, the aim here is to minimize the frequency and phase errors Δf_o and $\Delta \phi_e$, respectively, at the end of the frequency hop period t_{end} . The length of the frequency hop period and the maximum allowed phase and frequency error depend on factors such as system level specifications and telecommunication standards.

5.3 Synthesis of the optimum current waveform

The linear PLL model shown in Fig. 47. was used to find out the optimal waveform $i_1(t)$ which minimizes the phase error at the output during frequency transition in the speed-up method shown in Fig. 45. (a). Using the symbols shown in the figure, we can write the following equation for the phase error $\phi_e(s)$:

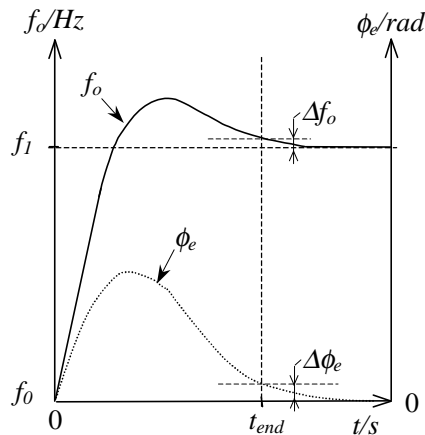


Fig. 46. Sample behaviour of output frequency and phase error during frequency transition.

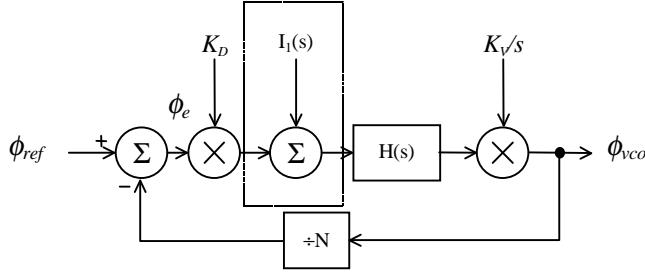


Fig. 47. PLL model used for $i_l(t)$ synthesis.

$$\phi_e(s) = \frac{\phi_{ref}(s) - \frac{1}{N} H(s) \frac{K_V}{s} I_1(s)}{1 + \frac{1}{N} H(s) \frac{K_V}{s} K_D}. \quad (33)$$

In the ideal case, the dynamic phase error would be zero during the transition. Consequently,

$$\phi_{ref}(s) - \frac{1}{N} H(s) \frac{K_V}{s} I_1(s) = 0, \quad (34)$$

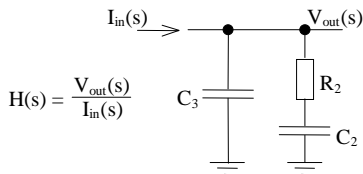
which leads to the following general equation for the optimal waveform in the s-domain:

$$I_1(s) = \frac{\phi_{ref}(s)}{\frac{1}{N} H(s) \frac{K_V}{s}} = \frac{N}{K_V} \frac{s}{H(s)} \phi_{ref}(s). \quad (35)$$

From now on it is assumed that the second order current-driven passive integrator shown in Fig. 48. is used as a loop filter. Such integrators are typically used in charge pump PLLs, and allow us to obtain the following loop filter transfer function:

$$H(s) = \frac{1 + s\tau_2}{s\tau_1} \frac{1}{1 + s\tau_3}. \quad (36)$$

The equations for the time constants τ_1 through τ_3 are presented in Fig. 48. Taking the inverse Laplace transform after substitution of (36) to (35) and assuming that $\phi_{ref}(s) = \Delta f / N s^2$ (equals a frequency step of Δf Hz at the output) we obtain - after some manipulation - the following equation for $i_l(t)$:



$$\tau_1 = C_2 + C_3 \quad (37)$$

$$\tau_2 = R_2 C_2 \quad (38)$$

$$\tau_3 = \frac{R_2 C_2 C_3}{C_2 + C_3} \quad (39)$$

Fig. 48. Second order passive integrator.

$$\Rightarrow I_1(s) = \frac{N}{K_V} \frac{s^2 \tau_1 (1 + s \tau_3)}{1 + s \tau_2} \frac{\Delta f}{Ns^2} = \frac{\Delta f}{K_V} \frac{\tau_1 (1 + s \tau_3)}{1 + s \tau_2} \quad (40)$$

$$\Rightarrow i_1(t) = \frac{\Delta f}{K_V} \frac{\tau_1}{\tau_2} \tau_3 D(t) + \frac{\Delta f}{K_V} \frac{\tau_1}{\tau_2} \left(1 - \frac{\tau_3}{\tau_2}\right) e^{-\frac{t}{\tau_2}}, \quad (41)$$

where $D(t)$ is Dirac's delta function. The part of equation (41) furthest on the left, i.e. Dirac's delta function and its multiplier, represents a charge which changes the voltage over the loop filter instantly to a new level at $t = 0$ s. It also alters the output frequency of the PLL to a value set by the gain factor of the VCO. However, the voltage over C_2 cannot change instantaneously due to resistor R_2 , which leads to a potential difference between the voltages across C_3 and C_2 . To reach a stable situation, the charge stored in C_3 starts to flow to C_2 through R_2 with the time constant $\tau_2 = R_2 C_2$. Therefore, an external replica of that current for $t > 0$, given by the part of equation (41) furthest on the right, must be delivered to the loop filter to keep both the voltage across the loop filter and the output frequency constant.

5.4 The problem of non-zero Δt

If one tried to realize the current waveform of equation (41), the Dirac's delta function would have to be replaced by a more practical pulse with finite width Δt , which leads to phase and frequency settling problems.

The first mechanism leading to a non-zero phase error after the initial charge pulse is due to normal PLL dynamics depicted in Fig. 49. (a). Mathematically the phase is the integral of frequency. As a consequence, frequency error in a PLL translates to phase

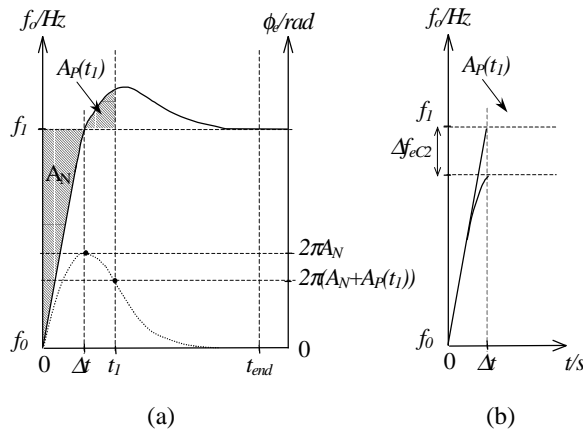


Fig. 49. (a) Build-up of phase error due to Δt and (b) frequency error due to current through R_2 .

error as shown in the figure. The phase error at Δt is directly related to the shaded area under the final output frequency f_l . This area results from the fact that during the initial current pulse from 0 to Δt the VCO input voltage grows linearly. A larger Δt produces a greater maximum phase error, i.e. larger A_N . To cancel out this phase error, the loop forces the output frequency larger than the final one. At that moment, i.e., when the areas below and above f_l are equal, the phase error goes to zero.

The second mechanism leading to phase and frequency fluctuations is caused by the current flowing through R_2 during the initial charge pulse. If Δt is not a good deal smaller than τ_2 , some of the initial charge delivered to the loop filter will flow to C_2 during $0 \leq t < \Delta t$. This makes the voltage across C_3 slightly smaller than expected, as shown in Fig. 49. (b), and the level of $i_l(t)$ after Δt slightly too high. However, normal PLL locking mechanisms will subsequently cancel out these errors. As explained in Paper XII, the speed-up waveform can be modified or two currents used to compensate for the charge transfer during and after the 1st charge pulse.

If the stringent condition used in equation (34) is relaxed, it is possible, for example using numerical methods, to find speed-up current waveforms which allow a controlled amount of phase errors to develop during speed-up, yet produce a faster settling. Nevertheless, it should be borne in mind that no great benefit can be gained by looking extensively for suitable waveforms with a high degree of complexity, because their accurate implementation with electrical circuitry would be difficult, especially when circuit imperfections are present. Therefore, a more straightforward speed-up waveform leading to a very simple $i_l(t)$ is proposed next.

5.5 The two-pulse method

In the two-pulse method, a predetermined amount of frequency error is used to speed up the cancellation of the accumulated phase error caused by the non-zero pulse width of the initial charge impulse and the normal operation of the loop. Fig. 50. shows the behaviour of the output frequency, the phase error and the shape of the speed-up signal for a slow loop ($i_2(t)$ refers to the current signal connected to C_2 in Fig. 45. (b)). The first charge

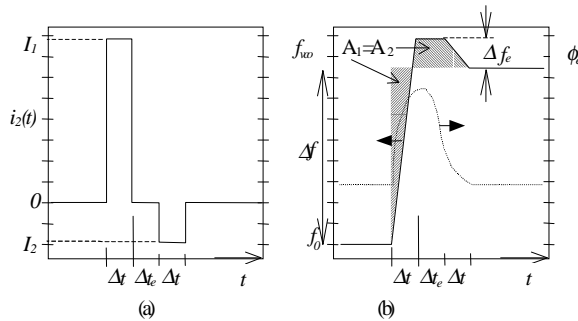


Fig. 50. Principle of the two-pulse method. (a) The speed-up signal and (b) output frequency and phase error.

pulse drives the VCO to a slightly higher frequency than the final output frequency. Because of the high frequency, the phase lag produced during the charge pulse is quickly reduced to zero (high frequency means more accumulated phases in a given time). Now, as the phase error reaches zero, a second charge pulse is used to set the VCO to the final output frequency. The required shape of $i_2(t)$ is very simple, namely, two current pulses with opposite direction and different magnitude. In terms of integration, this method is very attractive, since the additional circuitry is only required to produce very simple waveforms. The current waveform shown in Fig. 50. (a) was selected mainly, because it is easy to implement in practice and mathematically simple to model. However, the widths of the pulses and the position of the 2nd one could be selected differently without changing the basic idea behind the method.

Using a linear PLL model and assuming that C_3 and $i_1(t)$ in Fig. 45. (b) are both zero, thus turning the loop into a mathematically more manageable 2nd order system, the behaviour of the loop as a function of the current waveform parameters I_1 , I_2 and Δt can be derived. As a result of such analysis, the phase error after a frequency step at the input at $t = 0$ s is displayed in Fig. 51. (a). ($R_2 = 1.54$ k Ω , $C_2 = 22$ nF, $K_V = 8$ MHz/V, $K_D = 0.2$ mA/rad, $N = 104$, $\Delta f = 7.65$ MHz, $\Delta t = \Delta t_e = 1$ μ s). The curves exiting the graph at the top and bottom present the behaviour of the loop with a single current pulse applied at the beginning of the frequency hop. The curve labelled ‘no speed-up’ shows the unforced behaviour of the loop, which has intentionally been made very slow for added spurious suppression. As the height of the 1st pulse (I_1) increases, the phase error response bends more rapidly downwards. This is exactly what was intended by the initial current pulse – a very rapid phase error decay below zero. This decay rate can be increased by overdriving the output frequency of the loop as shown in Fig. 51. (b). Thus, the 1st current pulse increases the charge of C_2 sufficiently to provide the VCO with an input voltage which produces a somewhat higher output frequency than the final one.

The 2nd pulse is applied at $t = 2\mu$ s, and its effect is also shown in Fig. 51. The purpose of this pulse is twofold. First, it brings the output frequency exactly to the final value, thus zeroing the frequency error at $t = 3\mu$ s. Second, to avoid any frequency error after this point, the phase error must also go to zero at exactly the same moment. Thus, by properly selecting the magnitudes of the 1st and 2nd pulse – I_1 and I_2 , respectively – the phase and

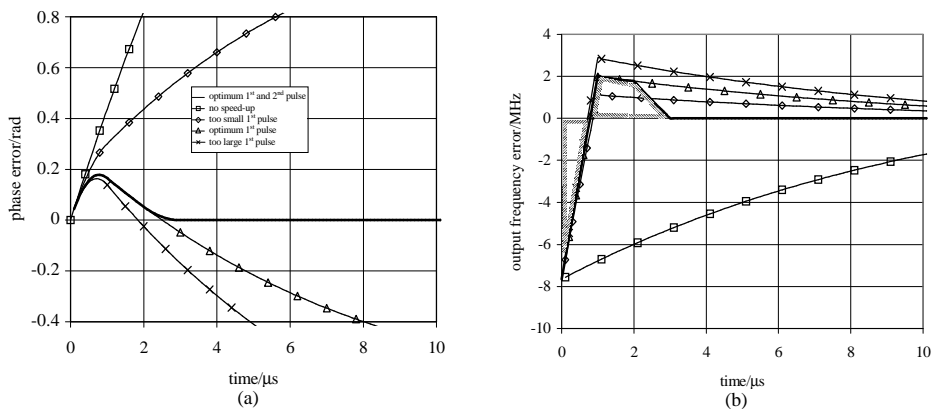


Fig. 51. (a) Phase error and (b) output frequency error after a step change in the input frequency for different speed-up waveforms.

frequency error are both completely cancelled out at the end of the 2nd pulse and any residual errors are avoided, as shown in Fig. 51. Qualitatively this means that the pulses force the areas inside the shaded boundaries in Fig. 51. (b) equal. As the sum of the areas (they have different signs) goes to zero, the phase error follows suit, since the phase error is proportional to the integral of the frequency error.

By setting the areas A_1 and A_2 in Fig. 50. (b) equal, a graphical analysis produces the following approximate formula for the speed-up waveform (i.e. pulse levels):

$$i_2(t) = \begin{cases} \frac{C_2(\Delta f + \Delta f_e)}{\Delta t K_V}, & 0 \leq t < \Delta t \\ -\frac{C_2 \Delta f_e}{\Delta t K_V}, & \Delta t + \Delta t_e \leq t < 2\Delta t + \Delta t_e \\ 0, & \text{otherwise} \end{cases}, \quad (42)$$

where parameters are as given in Fig. 50. and

$$\Delta f_e = \frac{\Delta f}{2(1+a)}, \quad (43)$$

where $a = \Delta t_e / \Delta t$.

The main problem with the use of the two-pulse method is the accuracy with which the zero phase error and zero frequency error can be reached simultaneously. If either error is non-zero at the end of the second current pulse, the loop reduces the remaining error to zero in accordance with normal loop dynamics. As the above equations do not take into account the dynamics of the loop, they give only a rough estimate of the correct pulse levels, and a numerical package or circuit simulation should be used to establish the precise values.

The speed-up method just analyzed in a 2nd order loop context can be applied to a typical 3rd order loop configuration of more practical frequency hopping RF synthesizers, if a second current source delivering a current

$$i_1(t) = \begin{cases} \frac{C_3(\Delta f + \Delta f_e)}{\Delta t K_V}, & 0 \leq t < \Delta t \\ -\frac{C_3 \Delta f_e}{\Delta t K_V}, & \Delta t + \Delta t_e \leq t < 2\Delta t + \Delta t_e \\ 0, & \text{otherwise} \end{cases}. \quad (44)$$

is added to the architecture, I_1 in Fig. 45. (b). This particular selection of $i_1(t)$ ensures that the voltage across R_2 will remain close to zero for all t . As a result, $i_2(t)$ will flow to C_2 alone, producing a proper voltage change at the input of the VCO and there will be no current flow through R_2 after the 2nd charge pulse. As shown in Fig. 52., a reasonably close match between the 2nd and 3rd order loops is achieved even when the optimum current levels I_1 and I_2 derived from the 2nd order loop are used as such.

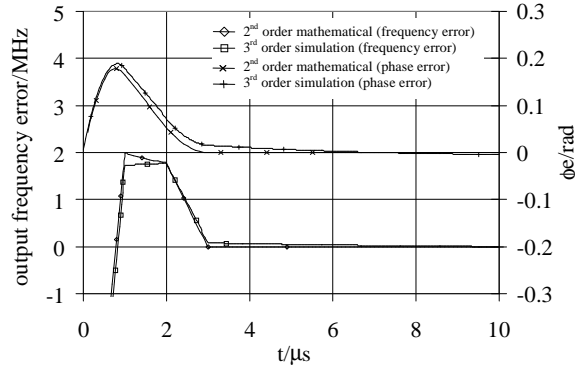


Fig. 52. Phase error and (b) output frequency error of theoretical 2nd order and simulated 3rd order loop.

The above discussion and mathematical formulations have been based on a linear loop with ideal loop parameters. Thus, throughout the previous paragraphs, the gain constants of the phase detector and the VCO were assumed fixed over the whole operating frequency range of the synthesizer, resistor and capacitor values were assumed to be known precisely at the design time, and pulse widths and rise times were assumed fixed. Unfortunately, none of these assumptions will be true in practice, which will lead to longer settling times than predicted.

Fortunately, in a practical realization of the two-pulse speed-up system, the loop itself may be used to compensate for VCO non-idealities, which is an obvious source of errors, when the optimum pulse levels are determined. In such a system the loop is used to characterize the VCO during operation by digitizing the VCO input voltage at each output frequency. However, this only compensates for VCO imperfections and not for loop filter component or PFD related unpredictability, which are not directly determinable from the DC voltage across the loop filter during normal operation of the synthesizer.

A possible implementation of such a speed-up system in an integrated form is depicted in Fig. 53. During normal operation of the synthesizer an analogue-to-digital converter

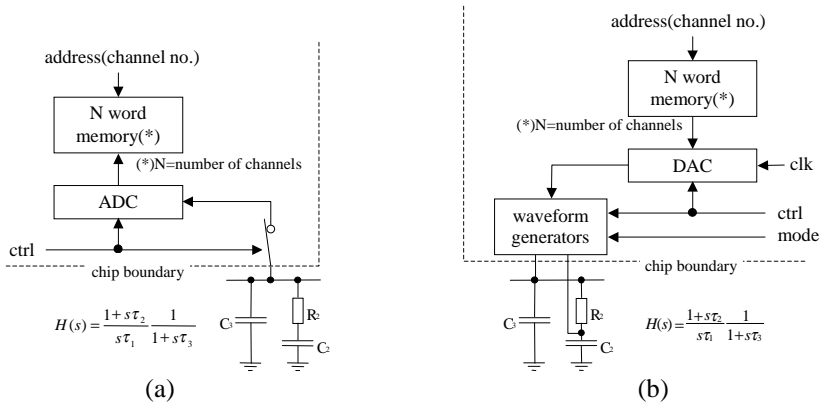


Fig. 53. Speed-up circuit during (a) normal operation of the synthesizer and (b) during frequency hop.

(ADC) samples the voltage across the loop filter and stores the value into digital memory. This operation is performed for each channel in the system (the number of channels may have to be restricted due to memory size limits), which will produce a memory table containing the approximate digital representations of the input voltage of the VCO for each channel (i.e. the f_{out} vs. V_{ctrl} characteristic of the VCO). Note that this table can be updated every time the synthesizer happens to operate in a given channel. Therefore, changes in operating conditions or aging, which affect the properties of the VCO, can at least in some degree be automatically compensated for.

The values in the memory table are used to calculate the correct pulse levels during speed-up, as depicted in Fig. 53. (b). A digital-to-analogue converter (DAC) re-produces the original voltage level corresponding the desired channel. This voltage level is used by the speed-up circuitry along with the current VCO input voltage to determine the magnitudes of the current pulses forced to the loop filter. Because the current levels needed to adjust the loop filter charge within the given speed-up period depends on the capacitance values of the loop filter, the current sources may have to be external. The entire speed-up circuitry with voltage sampling and production of the auxiliary speed-up signals can easily be designed in such a way that it works automatically in the background, without any involvement from the user.

5.6 Measurements

To test the ideas presented above, the measurement system shown in Fig. 54. was built around an existing PLL test board (PLL PCB). This circuit board utilizes a 800 MHz RF synthesizer ASIC (designed by the author), which contains all loop elements except the loop filter and the VCO. Different loop filters could easily be accommodated by the purpose-built on-board DIL socket. The circuit board is connected to a PC, which can be used to program the feedback divider ($\div N$) and the gain factor of the digital phase

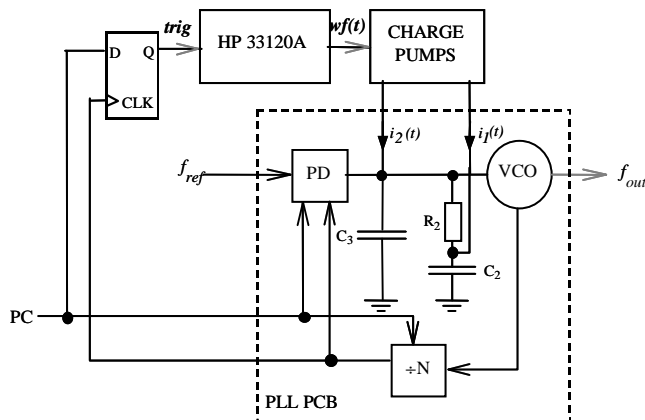


Fig. 54. The measurement setup built around an existing PLL PCB.

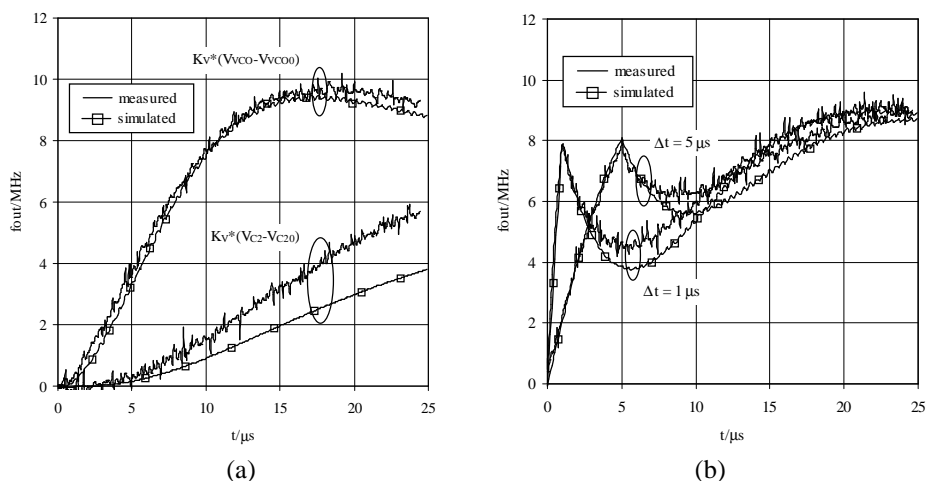


Fig. 55. (a) Frequency step response of the simulated and measured loop and (b) output frequency vs. time with single current pulse to the loop filter.

frequency detector with charge pump outputs (PD). The actual speed-up circuitry was built around an arbitrary waveform generator (HP 33120A) and a cascode current mirrors acting as charge pumps.

Fig. 55. (a) shows the measured and simulated (Matlab/Simulink) frequency step response of a loop with no speed-up of any kind ($\Delta f = 7.65$ MHz). Fig. 55. (a), like all figures containing measurement results, plot the voltage at the input of the VCO scaled by the gain of the VCO. The initial output frequency ($t < 0$ s) is subtracted from the results to make the x-scale more convenient. In the following discussion, the terms output frequency and VCO input voltage are used almost interchangeably due to this simple relation. All measurements were made using the 3rd order loop described earlier, and the results were compared to the Matlab/Simulink based simulation results of a 3rd order loop with realistic phase-frequency detector and divider models. Fig. 55. (a) also shows the voltage across capacitor C_2 , because it helps to explain most of the differences between the simulated and measured results. As can be seen, contrary to the curves representing the voltage at the input of the VCO, which match each other well, the curves showing the behaviour of the voltage across C_2 diverge. This difference between the simulated and measured results is mainly caused by the charge pump circuitry connected across C_2 , (e.g., finite output impedance and non-zero DC current before a charge pump induced frequency hop).

Fig. 55. (b) shows the response of the loop with a single charge pulse which brings the output frequency fast to the final frequency. In this measurement, only one current was connected to the loop filter, and, as a consequence, C_2 was not charged. As described earlier, this causes a voltage difference across the loop filter resistor and the subsequent loss of charge from C_3 to C_2 . This phenomenon can easily be recognized from the curves in Fig. 55. (b). After the initial charge, the curves representing the behaviour of the VCO output frequency dip towards the curve representing the behaviour of the voltage across C_2 . Fig. 55. (b) presents the curves for two different pulse widths, $1 \mu s$ and $5 \mu s$. The downward dip in the case of the $5 \mu s$ pulse is smaller, because the voltage difference

between the loop filter capacitors is smaller at the end of the pulse than in the case of the $1\ \mu\text{s}$ pulse. The reason for the differences between the simulated and measured results is the same – the voltage difference between the loop filter capacitors was smaller in the measurements, which lead to a reduced dip. The slightly exponential shape of the 1st rising edge of the $5\ \mu\text{s}$ pulse graphically displays the loss of charge to C_2 through R_2 during the charge pulse.

Fig. 56. displays the response of the loop after the loss of charge to C_2 after the initial current pulse has been compensated for by an exponentially decaying current signal. As expected, the rapid decay of output frequency evident in Fig. 55. (b) has been replaced by a flat region. In this case, the flat portion of the response is only six microseconds long, because practical reasons required that the exponential portion of the speed-up signal should be of this length. The dip after the flat portion is again caused by different voltages across the loop filter capacitors. The dip would become increasingly small, if the exponential portion of the speed-up current were extended further in time. However, as explained earlier, due to the phase error accumulated during the 1st rising edge of the frequency hop, some frequency overshoot produced by normal PLL action will occur when the magnitude of the speed-up current is sufficiently low compared to the output current of the PFD. As the theoretical review in the previous chapters did not include the effects of this current (the phase error was assumed to be zero due to the use of an ideal impulse), the magnitude of the exponential portion of the speed-up current had to be hand-tuned both in the simulation and during the actual measurements. Hand tuning during the experiments also accounted for the error between the simulated and measured loop responses explained above and shown in Fig. 55. (a). Thus, if the 1st current pulse is given a relative magnitude of one, the theoretical, simulated and measured values of the exponential portion at $1\ \mu\text{s}$ were 0.29, 0.24 and 0.20, respectively. The current predicted by the simple theory is too large, because it does not include two additional factors: the additional current component coming from the PFD and the faster-than-predicted decay of voltage error between the loop filter capacitors in the case of the sample loop.

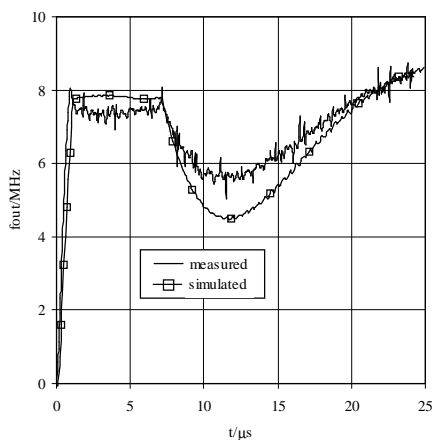


Fig. 56. Output frequency vs. time with a current pulse and exponentially decaying current to the loop filter.

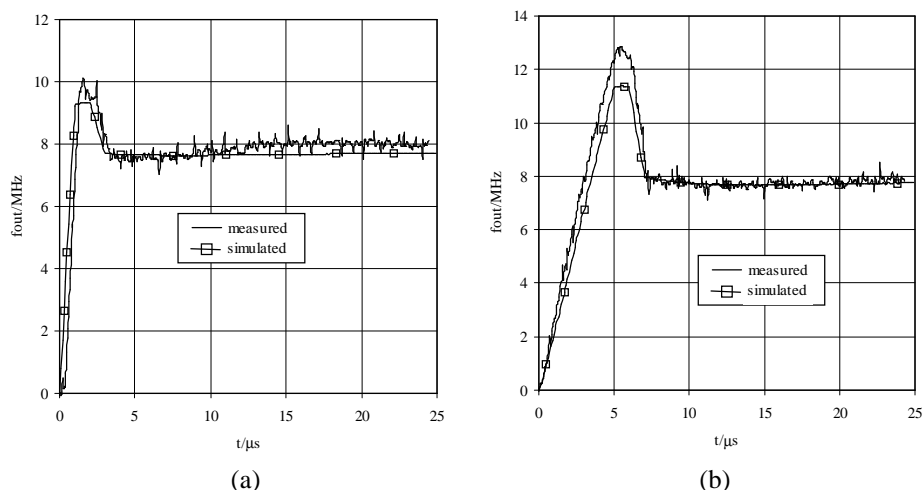


Fig. 57. (a) Output frequency vs. time when both current pulses of the two-pulse method are $1 \mu s$ long and (b) when the 1st pulse is $5 \mu s$ long.

Fig. 57. (a) shows the simulated and measured response of the loop using the proposed two-pulse speed-up method, which promises zero frequency and phase errors plus zero voltage across R_2 for a pulse width of $1 \mu s$ after a precisely selected time. Although their behaviour is almost ideal, differences between the simulated and measured loop cause small deviations. In the measurements, the speed-up waveform was produced by representing the magnitude of the 1st pulse as $+1.0000$ and, based on theory, the magnitude of the 2nd pulse was represented as a fraction of this value. Then the absolute current level was hand-tuned in order to end up at the final frequency at the end of the 2nd current pulse. Since the theory predicts that there is only one practical solution, i.e., only one set of pulse magnitudes, any errors in the transferred charge will result in a non-equilibrium state at the end of the speed-up waveform. This effect can be seen in the measured curve as a small overshoot after the end of the 2nd pulse. However, the maximum value of this overshoot at about $20 \mu s$ is still much smaller than the frequency overshoot of a loop without speed-up. According to the measurements, the magnitude of this overshoot can be reduced by scaling the current levels slightly too large. Thus, the output frequency will be slightly too high after the 2nd current pulse, whereafter the output frequency will quickly decay to the final value. A better result was also achieved, when the 1st pulse was made wider as in the case of the results shown in Fig. 57. (b) Peaking was considerably reduced with a $5 \mu s$ 1st pulse, a $1 \mu s$ pause and a $1 \mu s$ 2nd pulse. If the duration of the frequency step is defined as the time when the frequency error goes below the level where the normal and the speed-up loop response meet, the speed-up loop is seven times faster than the normal one.

As expected, the measurements indicate that the two-pulse method can be applied to real-life synthesizers. In practice, however, frequency errors can be completely cancelled only by fine-tuning the pulse levels. As a result, the usability of the two-pulse method is limited by the sensitivity of the final phase and the frequency error at the end of the frequency hop period to the levels of the current pulses (or more precisely, to the charge

transferred to and from the loop filter during the pulses). This sensitivity will be a function of the loop parameters, and its maximum allowed level depends on system specifications. In the presented case, for example, a frequency error of ± 12 kHz was produced by a $\pm 1\%$ error in the level of the 1st pulse. The figure agrees with that predicted by 2nd order loop approximation (± 17 kHz).

6 Discussion

The goal of this work was to develop integrated RF building blocks for base station transmitter and receiver architectures. Thus, the aim was to produce the same level of performance with custom integrated circuits as was previously produced by discrete or mixed discrete and integrated circuitry. Because of availability and cost reasons, the integration was done using standard BiCMOS processes. Because future transmitter and receiver architectures might differ greatly from the current ones, only those circuit functions which also have use in the future, were selected for study, namely I/Q modulator, 90° phase shifter, variable gain amplifier and synthesizer. Several test chips were designed and measured. It was shown that useful integrated structures can be developed for the base station environment.

The base station of a modern telecommunications system provides special boundaries to the design of integrated RF structures. On the other hand, specifications of individual circuit blocks are tight due to system level specifications and the nature of the application – i.e. if the base station fails, the whole system fails. However, base station environment relaxes power consumption and size requirements, which makes the choice of an overall architecture more flexible. Therefore, the complete integration of transmitter and receiver RF parts is not the best way to go in a base station, but a mixed technology, mixed discrete and IC design will provide the best performance. Thus, the most obvious circuit functions for integration using standard BiCMOS processes are those studied in this thesis, and not for example power amplifier or low-noise amplifier, which can be most conveniently realized by using GaAs based technologies.

A typical BiCMOS process was used to realize the main circuits because of cost and speed reasons. The cost was kept under control because the selected processes were not optimized for RF design and were not most advanced with respect to the minimum line width. An even cheaper CMOS process could not be used because MOS transistors alone did not accommodate the high-speed signal processing. The I/Q modulator and variable gain amplifier circuits could also have been made with a pure BJT process, although these processes are not as readily available and are often more expensive. For the synthesizer designs, BiCMOS was naturally the preferred technology, because these circuits contain both low-frequency digital logic (CMOS) and a high-frequency prescaler (CML/ECL).

In the circuits described in this work, the maximum signal frequency which could be handled was limited by the transition frequency f_t of the BJT transistors. The transition

frequencies of the 1.2 μm and 0.8 μm double poly/double metal BiCMOS processes used here were 8 GHz and 12 GHz, respectively. Therefore, these processes could accommodate the maximum operating frequency of 2 GHz (synthesizers). However, the maximum f_i occurs only at a certain emitter current density, which automatically sets the current level of each transistor stage of the highest frequency circuit structures. In these processes the maximum f_i of the smallest transistor occurs with emitter currents in the neighbourhood of 500 μA . This quite large minimum current per transistor stage is the principal reason for the large power consumption of the realized circuits, especially when transistors were scaled up due to noise and matching reasons.

As the layout design and packaging of RF-ICs is of great importance, the guidelines given in chapter 3 were followed as much as possible. The package parasitics were taken into account early on in the design cycle and cross-coupled structures with dummy devices were used extensively. The smallest possible package was always used, however, since test circuits like these often have extra I/O for characterization purposes, which make the package larger than actually needed. Sensitive circuit blocks were dedicated their own supply pins, and supply voltages and differential signals were connected to the chip as explained in Chapter 3. Test pads were included in many designs to facilitate the characterization of individual circuit structures or for error tracking. Differential structures and protection structures were used as often as possible for increased noise rejection.

An I/Q modulator with adequate performance was designed and its operation verified by measurements. Extensive measurements covering the whole operating conditions range prove that the designed circuit fulfills the LO suppression and image rejection specifications in most situations. Two 90° phase shifter topologies were tested – one analogue and one digital. The digital phase shifter proved to possess a better overall performance with an accuracy sufficient to provide image rejection according to the specification (-35 dBc) over the whole operating conditions range (4.5 – 5.5 V/-10 – +85°C). Special attention was paid to the layout design (e.g. cross-coupled structures, dummy devices, protection structures). Thus, the measured LO suppression exceeds the specifications (-35 dBc) at all operating conditions except at extremely high temperatures.

The comparison of the developed circuits to those reported in the literature is difficult, because the modulators here were developed for a given application using a given process and exact predesign knowledge of signal levels, for example. The comparison is further hindered because most similar designs only report some of the parameters at nominal operating conditions. This is especially true for I/Q modulators, which are integrated as part of the complete transceiver ASIC. Additionally, the designs differ with respect to operating frequencies, signal levels and the process being used – e.g. the availability of inductors and highly resistive substrate have a great influence on many performance parameters. However, a brief summary of similar designs, i.e. direct up-conversion I/Q modulators is presented in Table 7. The results reported in this thesis are quite comparable to the results of both academic and commercial designs shown.

A DC to 1.5 GHz variable gain amplifier (VGA) was realized with a linear 50 dB gain adjustment range, maximum gain of 18.5 dB and gain variation of 1 dB up to 700 MHz over the whole operating conditions range of $V_{CC} = 4.5 \dots 5.5 \text{ V}$ and $T = -10 \dots +85 \text{ }^\circ\text{C}$, which provides performance comparable to those required for direct transmitter applications in the GSM base station.

Table 7. Performance of various I/Q modulators.

Circuit	Pout [dBm]	LO Suppression [dBc]	Image rejection [dBc]	Phase shifter accuracy [deg.]	PDC [W]	Size [mm ²]
Imai & Kikuchi (1992)	N.A.	N.A.	N.A.	±0.3(1)	0.25	2.5x1.5
Steyaert & Roovers (1992)	-40(2)	32	N.A.	±3.0	0.12	1.8x0.5
Bóveda et al. (1993)	N.A.	40	40	5/1(3)	0.6	2.2x2.4
Tsukahara et al. (1996)	20	> 40	> 35	2	0.068	2.4x0.68
Fenk et al. (1990)	0	43	43	±2.0	(7)	N.A.
Kazin et al. (1998)	-2.52	30.48	48	N.A.	N.A.	N.A.
Stetzler et al. (1995)	0	32	40	1.0	N.A.	N.A.
Djen & Shah (1994)	1.70	> 40	> 40	N.A.	N.A.	N.A.
HPMX-2003 (Hewlett Packard 1993)	6	36	36	1.25	0.18	
SA900 Philips Semiconductors (1994)	2	45/35(4)	45/35(4)	1.2(5)	0.3	
Modulator with digital phase shifter (IV, V)	-15(6)	45	37	±1.0	0.5	2.0x2.0

(1) at 200 MHz, (2) from a figure, (3) with and without tuning, (4) typ./min., (5) IR = 40 dBc, modulator only a part of the chip, (6) at 948 MHz, (7) 40 mA (supply voltage not given)

The comparison of the designed variable gain amplifier circuits to those reported in the literature is difficult. First of all, most of the reported VGA designs are meant for receiver applications, where the requirements of the VGA are different. For example, the receiver VGA must provide more gain due to noise reasons than the transmitter VGA and the compression specifications of the transmitter VGA have to take into account not only the signal of interest but also the potentially much stronger signals in the adjacent channels. Contrary to this, the transmitter VGA processes only one well-known signal, the properties of which can be accounted for during design. Second, most of the reported VGAs operate at intermediate frequencies, thus direct comparison to a 1 GHz VGA is not possible. Furthermore, because of the lower operating frequency, the reported designs often utilize CMOS technology. (Tadjpour (1998), van Lieshou & van de Plassche (1997), Pan & Abidi (1989).)

For comparison purposes, some of the most closely resembling VGA designs reported in recent literature are summarized in Table 8 (Hauptmann et al (1992), Reimann & Rein (1989), Meyer & Mack (1991), Sansen & Meyer (1974), Song et al. (2000), Otaka et al. (2000), Djen & Shah (1994), Shin et al. (2000)). The comparison is somewhat crippled since it is typical nowadays to incorporate VGA amplifiers into integrated transmitter structures without reporting a complete set of VGA specific performance parameters (e.g. Djen & Shah (1994)). Most often the only nonlinearity parameter given for transmitter VGAs is the compression power, since mixing of several input signals through nonlinearities is not the main problem. Due to the strong input signal, the noise properties of transmitter VGAs are also rarely given. To sum up, it can be stated that the VGA circuits developed in this work perform as required by the application and comparably to other similar designs when the overall performance is considered and differences in processing are taken into account (i.e. differences in the power consumption).

The synthesizer circuits developed during this work were targeted to the RF frequency synthesis applications in the GSM base station. However, the specific application was such that the frequency step was not the usual 200 kHz but rather 10 MHz or 20 MHz, thus providing rougher frequency steps. This makes it difficult to compare the synthesizers to those presented in the literature. Besides, many of the performance parameters of a synthesizer can be set by the properties of the loop filter, which are often not given. Additionally, second order effects such as spurious signals depend strongly on the reference frequency, loop filter bandwidth and the quality of the measurement system (e.g. isolation properties of the test PCB).

One way to compare synthesizer designs is to use the concept of 1 Hz normalized phase detector noise floor, as defined by Banerjee (1998), for example. When this concept is used, the phase noise performance of synthesizers using different reference frequencies and feedback dividers can be compared. Besides, this measure describes exactly the quality of those loop components integrated in the synthesizer ASICs designed in this work and is independent of the VCO properties, for example. This facilitates direct comparison of different loops whether the VCO is integrated in the same chip in conjunction with the rest of the loop components or not. Banerjee (1998) also reports the 1 Hz Normalized Phase Detector Noise Floor of various National PLLs, which are

Table 8. Performance of various VGAs.

Circuit	Gain adj. range [dB]	Frequency of operation [MHz]	Output TOI [dBm]	Output -1 dB compression power [dBm]	PDC [mW]	Size [mm ²]
Hauptmann et al. (1992)	15	< 0.0034	N.A.	N.A.	1.7	0.8
Reimann & Rein (1989)	40	2500	N.A.	N.A.	768	1.5x2.7
Meyer & Mack (1991)	30	1000	+13.5	-3.0 ⁽⁴⁾	225	1.27x1.02
Song et al. (2000) ⁽¹⁾	100	< 200	> -10	N.A.	32.4	0.58x0.66
Otaka et al. (2000) ⁽²⁾	70	< 500	+5	N.A.	36.0	1.0
Djen & Shah (1994) ⁽³⁾	40	836.00	N.A.	N.A.	N.A.	N.A.
Shin et al. (2000)	89	130.38	N.A.	+4.7	18...72	0.75x0.65
Basic VGA (IV)	50	960	+10.48	+3.1	200	1.15x2.15

(1) CMOS, (2) receiver VGA, (3) part of a complete transmitter ASIC, (4) at 100 MHz

compared in Table 9 combined with some other synthesizers to one of the designs reported in this thesis. Once again the phase noise performance of the developed synthesizers is comparable to those reported elsewhere.

One of the main problems with integer-N PLL based synthesizers, when used in multiple channel systems, is the level of spurious signals at the output of the synthesizer when the speed of the loop is optimized for fast frequency switching. Therefore, different means to accelerate the frequency hop when the loop is made narrowband for additional spurious attenuation were investigated. The literature already reports many ways to increase the speed of the loop during the frequency hop, but rarely in the context of loops having frequency hop time around 10 μ s and the frequency hop magnitude around 10 MHz. Conventional methods, such as loop component and PFD output current switching were briefly tested. However, the main contribution of this thesis in this area is the study of speed-up methods where the charge of the loop filter is directly controlled by external current or voltage signals.

The aim in this work has been to develop a method to make the frequency step response of a phase-locked loop faster using current or voltage waveforms to control the charge stored in the loop filter during the frequency transient. The increased speed could later be traded off to a lower output spurious signal by lowering the closed loop bandwidth of the loop. In this thesis integer-N PLL based synthesizers with a second order passive integrator as the loop filter are specifically considered.

In the kind of PLL considered here, the time at which the loop reaches the final equilibrium after a frequency step is dependent on three conditions which must be met simultaneously. These conditions are: 1) frequency error must be zero, 2) phase error must be zero and 3) the voltage across the loop filter capacitors must be equal. The purpose of the signal superimposed on the loop filter is to help the loop to reach these conditions faster than normally.

If the speed-up signal is a current signal connected across the loop filter, the optimum waveform is easily found using a linear PLL model. This signal consists of a charge

Table 9. 1 Hz Normalized Phase Detector Noise Floor for Various PLLs.

	PLL	1 Hz Normalized Phase Detector Noise Floor (dBc/Hz)
Banerjee (1998)	LMX233x	-211
	LMX233xL	
	LMX23x6 single	-210
	LMX15x1,23x5	-206
	LMX2350/52	-201
	LMX 1600 family	-199
	Lo et al. (1998)	-198
	Craninckx & Steyaert (1998)	-185
	Lin (2000)	-221
	Synthesizer 2 (IX)	-210

impulse, which switches the output frequency instantly to the new value, and of an exponentially decaying current, which provides the charge needed by the loop filter capacitors to reach the same potential without disturbing the VCO input voltage. Since the frequency is switched to the new value infinitely fast, no phase error occurs in the loop. Thus, after the initial charge impulse, conditions 1 and 2 are met and the 3rd condition is reached later in such a way that the loop thinks that the final equilibrium is also reached instantly. Unfortunately, an ideal impulse cannot be generated in practice, which makes this theoretical waveform impractical.

Because phase error is the integral of frequency error, any practical speed-up method, which does not change the frequency instantly to the final new one will allow some phase error develop in the loop. Thus, in order to meet the above-mentioned 2nd condition, some frequency error must also occur through the normal loop operation or by additional speed-up action. Therefore, a direct hop to the new frequency is not possible when the loop filter charge is controlled by a charge pulse with a finite width rather than impulse.

A method using only two relatively wide current pulses, which in theory provide the possibility to achieve all of the above-mentioned conditions simultaneously, is proposed. In this method the output frequency is first changed with a current pulse to a non-equilibrium value, which provides rapid reduction of the phase error to zero. As the phase error goes to zero, the frequency is changed to the final value with a second current pulse. When appropriately scaled copies of the current pulses are delivered to both of the loop filter capacitors, all conditions leading to the final equilibrium are met at the end of the second current pulse.

The operation of the speed-up systems using the developed waveforms were verified by measurements. An arbitrary waveform generator was used as the waveform source driving discrete charge pumps connected to an existing RF-IC synthesizer with $f_{\text{out}} \approx 800$ MHz and the frequency step time in the tens of μs range was used as the test application. Comparison of mathematical, simulated and measured results show that simple current pulses can indeed be used to speed up the channel switching of a practical RF synthesizer. In the example, with the given definition of the frequency step length, the ratio between the normal and the speed-up step length was seven to one. However, the advantage gained depends heavily on loop properties, how accurately the speed-up waveforms can be generated and what the definition of the frequency hop period is. Here the length of the hop was simply defined as the time between the beginning of the frequency transition and the point in time at which the free response of the loop and the speed-up response meet. The dependence of the speed-up advantage on loop parameters and specifications makes the comparison of the presented speed-up method to other reported speed-up methods difficult. It also seems that none of the reported methods comes with a direct formulation of how to predict the performance improvement offered by the method when used in a loop with arbitrary loop parameters.

In the future the operation of the proposed speed-up method must be verified using a real-life synthesizer as the target application. In this way it will be possible to find out how much benefit the proposed method can offer in a specific application. Another interesting idea is the combination of $\Delta\Sigma$ driven fractional-N synthesizer with the proposed speed-up method, which might lead to the ultimate goal of a very high-speed spur free synthesizer.

7 Summary

The thesis concentrates on the practical realization of the fundamental building blocks of different RF architectures in the base station environment. Several circuits performing different RF operations are designed and tested. The main emphasis here is to provide the same level of performance as with existing discrete and mixed discrete/integrated designs.

The common RF building blocks are identified by reviewing different transmitter and receiver architectures. Structures such as low-noise amplifiers, power amplifiers, synthesizers, mixers and filters are common to all architectures, whether built in a more traditional discrete form or as an integrated circuit. Not all of these basic circuit structures are suitable for integration especially in base station environment where there is no need to trade performance for a smaller area or power consumption. Therefore, the emphasis in this thesis is not in the integration of the whole transceiver circuitry but rather in the efficient realization of building blocks fit for integration. This excludes optimised LNA and PA structures using discrete devices and external high-frequency filters. This leaves mixers, especially quadrature mixers specific to vector modulated systems, and frequency synthesizers that are always present in multichannel systems as the main targets of interest.

One of the main topics of this thesis is to develop a method to make the frequency step response of a phase-locked loop faster using simple current waveforms. The increased speed could later be traded for lower closed loop bandwidth, thus alleviating the spurious problem of integer-N PLL synthesizers.

A method using only two current pulses to speed up the frequency step response of the loop is proposed. These pulses are produced by a current generator connected to the loop filter. In the proposed method the output frequency is first changed with a current pulse to a non-equilibrium value, which provides rapid reduction of the phase error to zero. As the phase error goes to zero, the frequency is changed to the final value with a second current pulse, thus leading to the final equilibrium.

The basic operation of the proposed speed-up method was verified by measurements. An existing RF-IC synthesizer designed as part of the work presented here with $f_{\text{out}} \approx 800$ MHz and the frequency step time in the range of tens of μs was used as the test application. The comparison of mathematical simulated and measured results show that simple current pulses can be used to speed up the channel switching of a practical RF

synthesizer. In the example, the frequency step length was made seven times shorter using the proposed method.

Several circuit implementations were developed using mainly 0.8 and 1.2 μm full custom BiCMOS processes. The main circuit structures and their measured properties are: 90° phase shifter with $\pm 1^\circ$ phase error with $V_{CC} = 4.5 \dots 5.5$ V and $T = -10 \dots +85$ °C, I/Q modulator suitable for operation at output frequencies from 100 MHz to 1 GHz and baseband frequencies from 60 to 500 kHz (2.0 mm x 2.0 mm, 100 mA, 5.0 V) with LO suppression of 38 dBc and image rejection of 41 dBc, temperature compensated DC to 1.5 GHz variable gain amplifier (1.15 mm x 2.00 mm, 100 mA, 5.0 V) with a linear 50 dB gain adjustment range, maximum gain of 18.5 dB and gain variation of 1 dB up to 700 MHz over the whole operating conditions range of $V_{CC} = 4.5 \dots 5.5$ V and $T = -10 \dots +85$ °C, a complete bipolar semicustom synthesizer (90...122 mA, 5.0 V) and three complete full-custom BiCMOS synthesizer chips including all building blocks of a PLL-based synthesizer except for the voltage controlled oscillator and the loop filter. The synthesizers include circuit structures such as ~ 2 GHz multi-modulus divider and low-noise programmable phase-detector/charge-pump ($18.7 \text{ pA}/\sqrt{\text{Hz}}$ at $I_{\text{out}} = 500 \text{ }\mu\text{A}$) and have an exemplar phase noise performance of -110 dBc/Hz at 200 kHz offset.

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